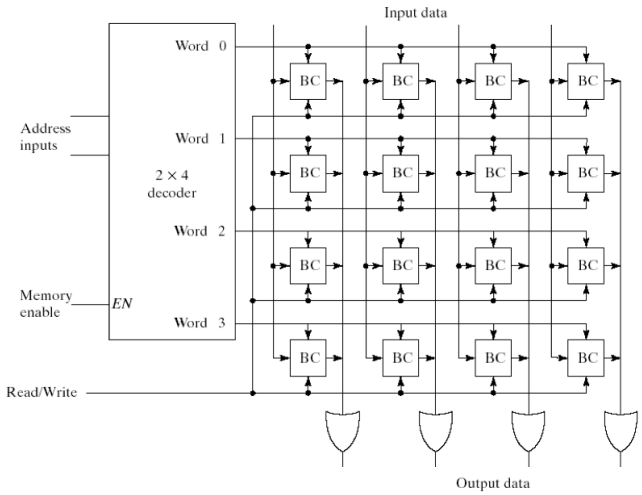
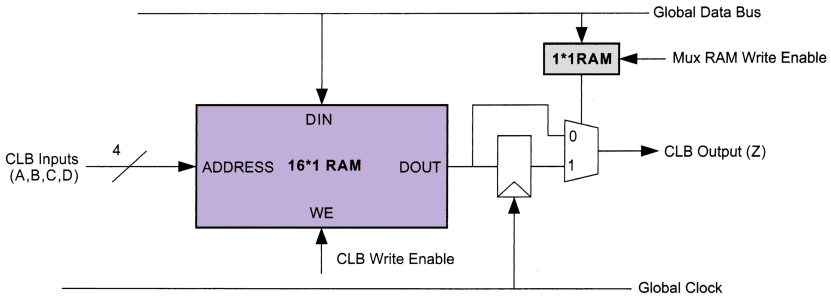
HW7

1. (10%) The memory units are specified by the number of words times the number of bits per word. (1) How many address lines and input-output lines are needed in each case? (2) Give the number of bits stored in the memories in each case. (a) 2M x 16 (b) 32K x 4.
2. (20%) A 4x4 RAM below shows all inputs and outputs. Assuming three-state outputs, construct an 8x8 memory using the four 4x4 RAM units. (Hint: Similar to decoder size extension in decoder with enable input.)



3. (20%) A 12-bit Hamming code word containing 8 bits of data and 4 parity bits is read from the memory. What is the original 8-bit data word that was written into memory if the 12-bit word read out is as follows: (a) 011001000110 (b) 101110110100.
4. (14%) A 64K × 4 RAM chip uses coincident decoding by splitting the internal decoder into row select and column select.
   (1) Assuming that the RAM cell array is square, what is the size of each decoder and how many AND gates are required for decoding an address?
   (2) Determine the row and column selection lines that are enabled when the input address is the binary equivalent of $(880)_{10}$.
5. (20%) A simple FPGA logic cell is shown as figure below:
   (1) (10%) Explain how the logic cell can implement the sum function in a full adder. (Z=A+B+C)
   (2) (10%) Explain how the logic cell can implement a 1-bit T-type flip-flop function.



6. (16%) Tabulate the truth table for an 8x4 ROM that implements the Boolean functions.
   (1) A(X, Y, Z) = Σm(1, 3, 5)
   (2) D(X, Y, Z) = Σm(2, 3, 5, 6, 7)

