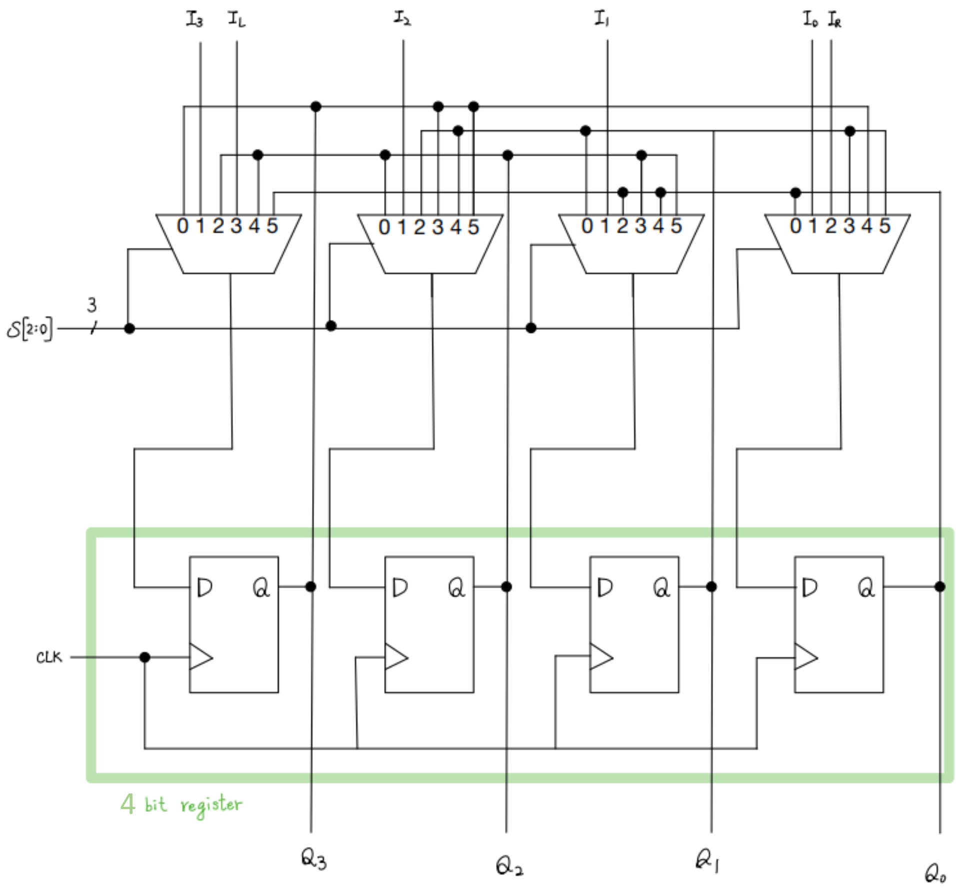
Logic Design HW6 Solution

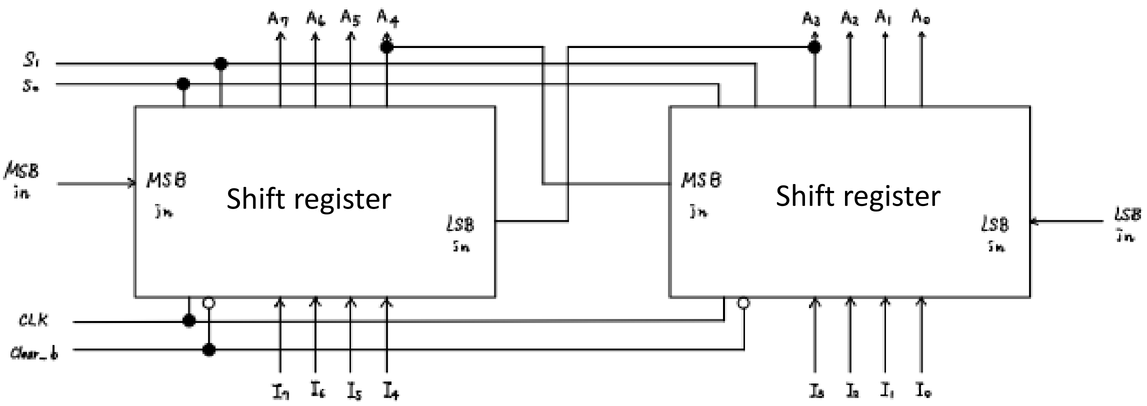
1. **(20%) Using a 4-bit register, construct a 4-bit shift register that can shift/rotate its content one position to the left or right**



MUX	S2	S1	S0	Operation
0	0	0	0	No operation
1	0	0	1	Load input
2	0	1	0	Shift left
3	0	1	1	Shift right
4	1	0	0	Rotate left
5	1	0	1	Rotate right

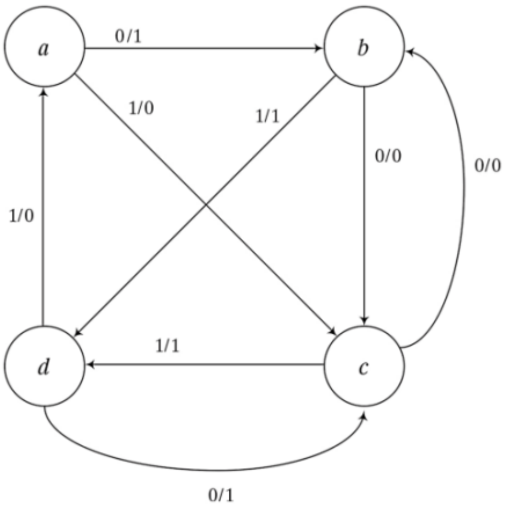
2. **(20%) Construct an 8-bit universal shift register from 4-bit registers as shown below.3.**

S0	S1	Operation
0	0	No change
0	1	Shift right
1	0	Shift left
1	1	Load input

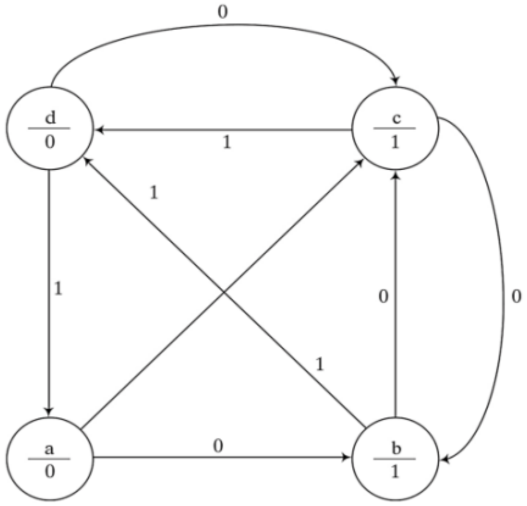


3. (20%) For the following two state diagrams, identify the Mealy Machine and Moore Machine, respectively. Prove or disprove that they are equivalent.

Mealy Machine



Moore Machine



State	Input	Next state	Output
a	0	b	1
a	1	c	0
b	0	c	0
b	1	d	1
c	0	b	0
c	1	d	1
d	0	c	1
d	1	a	0

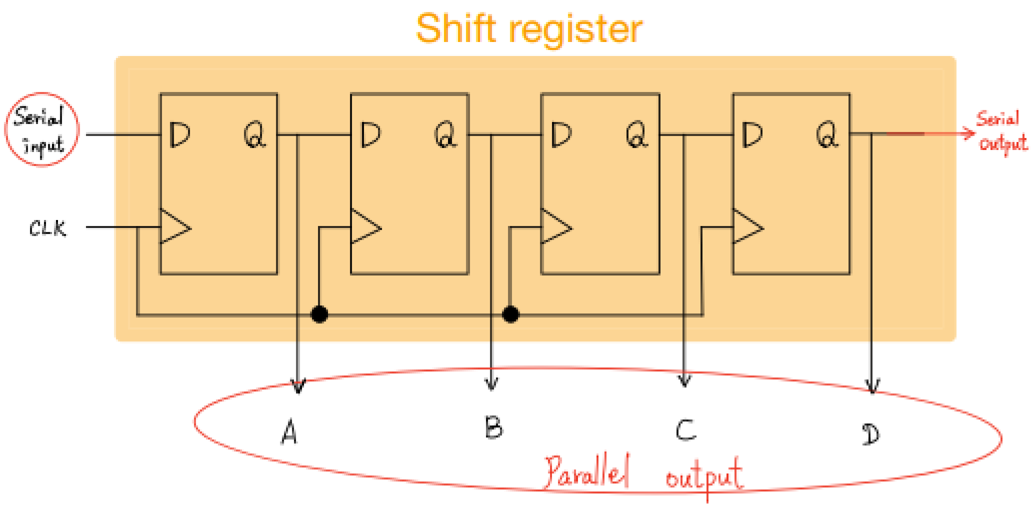
State	Input	Next state	Output
a	0	b	0
a	1	c	0
b	0	c	1
b	1	d	1
c	0	b	1
c	1	d	1
d	0	c	0
d	1	a	0

They are not equivalent

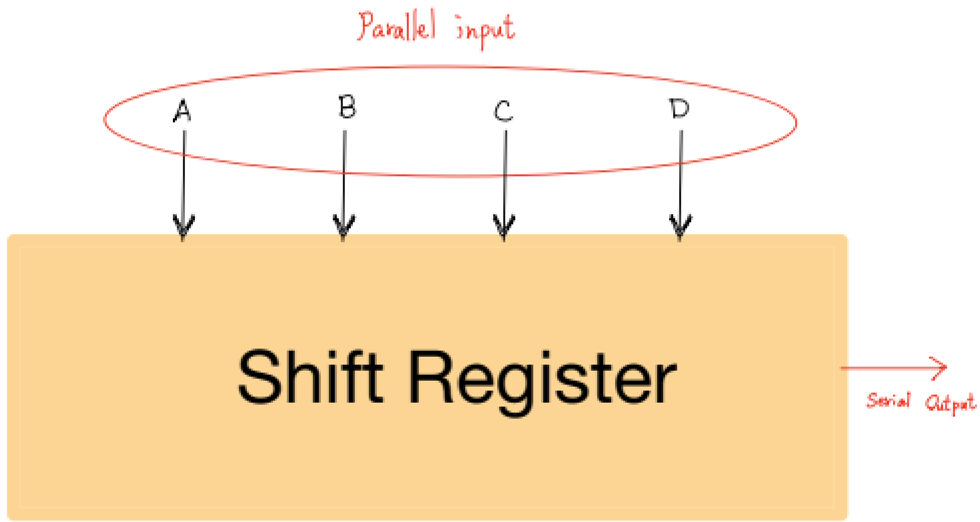
4. (10%) What is the difference between serial and parallel transfer? Explain how to convert serial data to parallel and parallel data to serial. What type of register is needed?

Serial transfer	Data transmit in order, time↑, area ↓
Parallel transfer	Data transmit simultaneously, time↓, area ↑

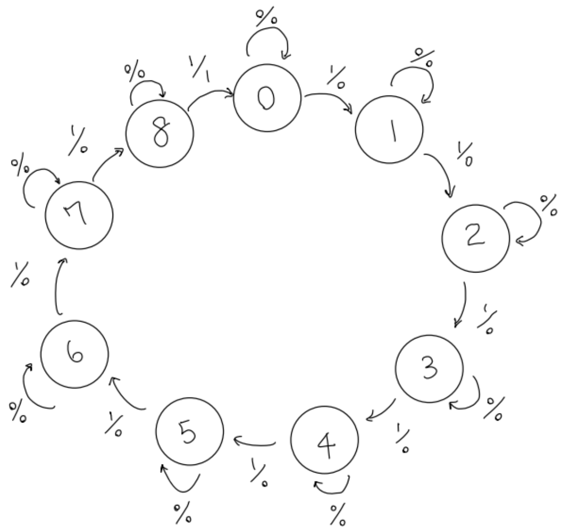
Serial to parralel



Parallel to Serial

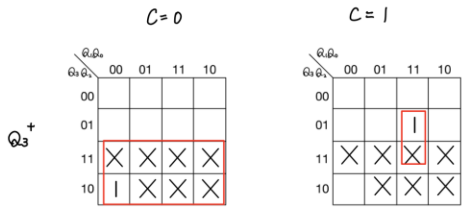


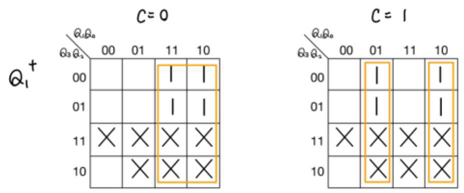
5. (15%) Design a modulo-9 counter using D FFs, with the counting sequence (0, 1, 2, 3, 4, 5, 6, 7, 8, 0, 1, ...), which produces y = 1 if the state '8' is encountered (i.e., when we go from state '8' to state '0'), and y = 0 otherwise. The counter stays in its current state iff C = 0, and makes state transition iff C = 1. You can use only D FFs. Show the state diagram and minimized state table, then derive the simplified output and excitation functions. Finally, show the schematic.

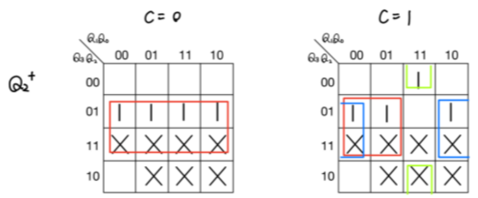


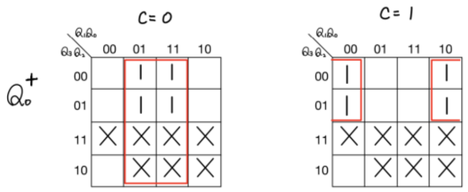
Present State					Next State		Output (y)	
	Q_3	Q_2	Q_1	Q_0	C=0	C=1	C=0	C=1
0	0	0	0	0	0000	0001	0	0
1	0	0	0	1	0001	0010	0	0
2	0	0	1	0	0010	0011	0	0
3	0	0	1	1	0011	0100	0	0
4	0	1	0	0	0100	0101	0	0
5	0	1	0	1	0101	0110	0	0
6	0	1	1	0	0110	0111	0	0
7	0	1	1	1	0111	1000	0	0
8	1	0	0	0	1000	0000	0	1

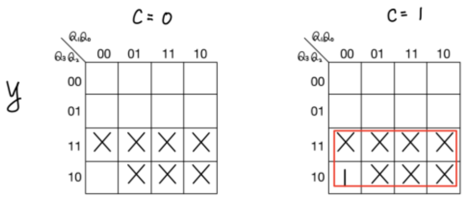
K-Map :











$Q_3 = Q_3C' + Q_2Q_1Q_0C$

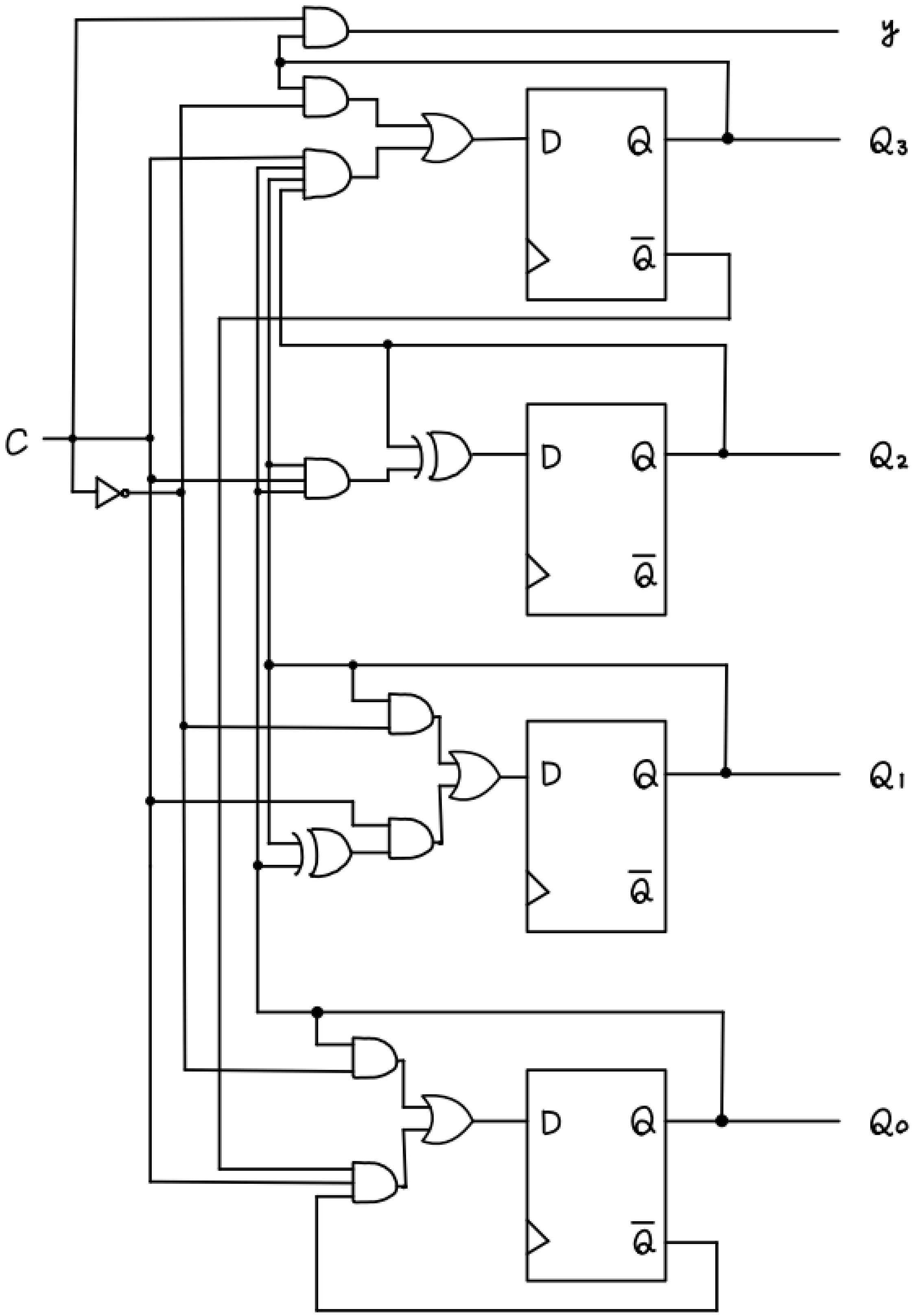
$Q_2 = Q_2Q_1' + Q_2C' + Q_2Q_0' + Q_2'Q_1Q_0C = Q_2 \oplus Q_1Q_0C$

$Q_1 = Q_1C' + Q_1Q_0'C + Q_1Q_0C = Q_1C' + C(Q_1 \oplus Q_0) = Q_1C' + C(Q_1 \oplus Q_0)$

$Q_0 = Q_0C' + Q_3'Q_0'C$

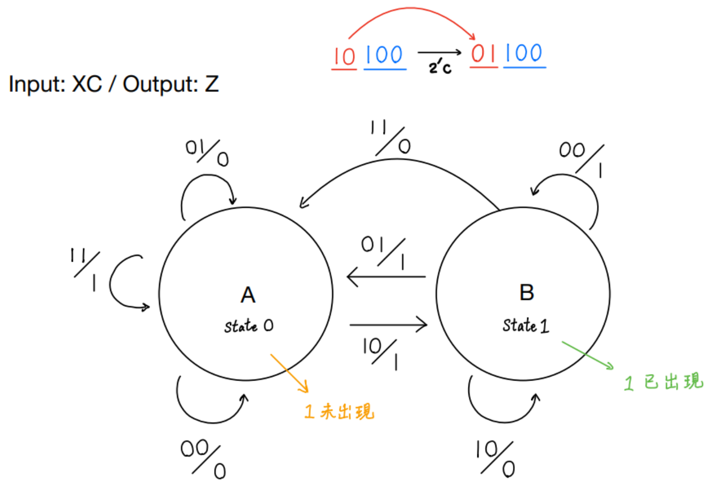
$y = Q_3C$

Circuit diagram:



6. (15%) We are going to design a serial two's-complementor circuit using D FFs. A binary integer of arbitrary length is entered into the input X of the two's-complementor, with LSB first. When a given bit is entered on input X, the corresponding output bit is to appear during the same clock cycle on output Z. When the other input C becomes 1 for one clock cycle, it indicates that a sequence is complete and that the circuit is to be initialized to receive another sequence. Otherwise, C = 0. Give the state diagram and state table for the serial two's-complementor, and follow the design procedure step by step to obtain a circuit implemented by D FFs.

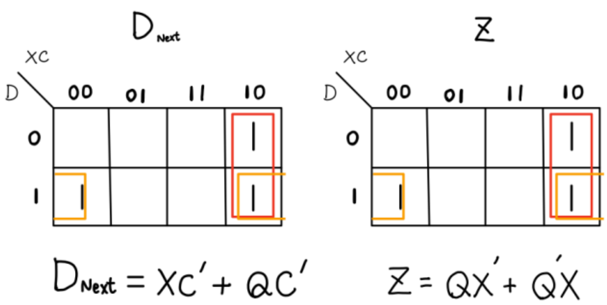
State diagram:



State table:

Present State	Next State D_{Next} / Z			
D	XC=00	XC=01	XC=10	XC=11
0	0/0	0/0	1/1	0/1
1	1/1	0/1	1/0	0/0

k-map:



Circuit diagram: