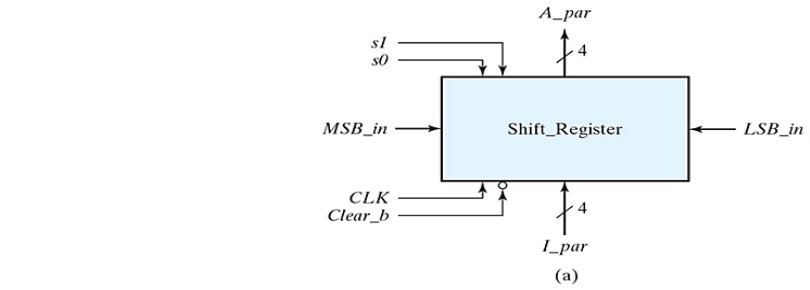
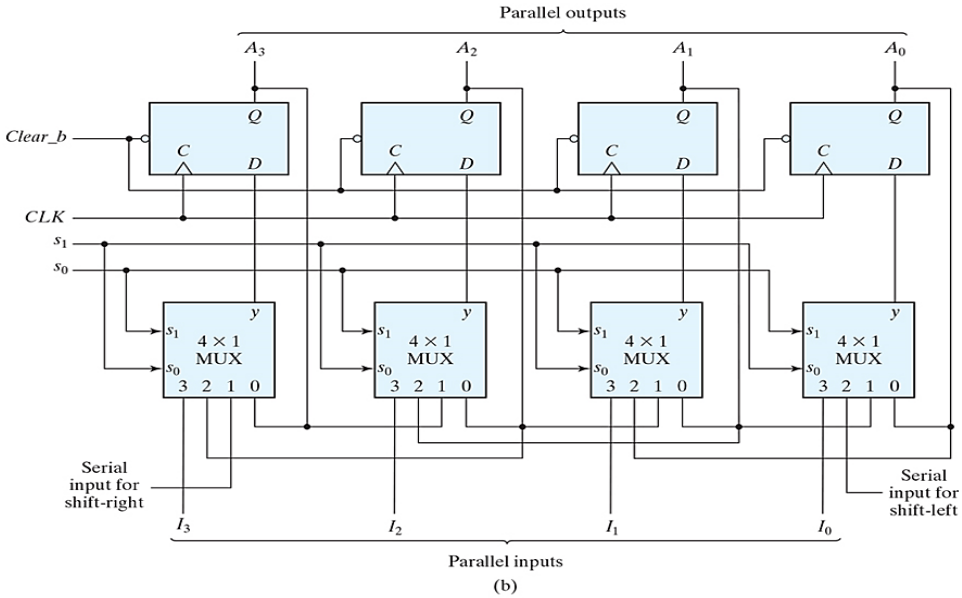
Homework #6

Due **13:20** on 12/23 (Thu)

1. (20%) Using a 4-bit register, construct a 4-bit shift register that can shift/rotate its content one position to the left or right.
2. (20%) Construct an 8-bit universal shift register from 4-bit registers as shown below.

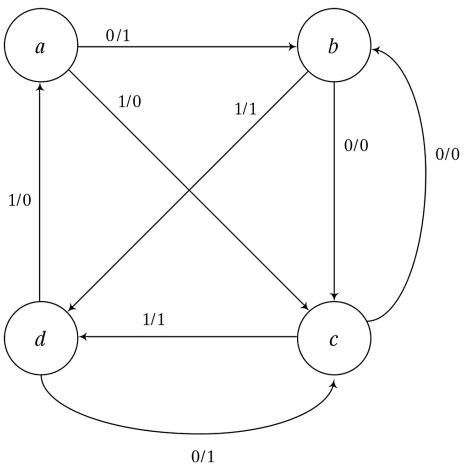


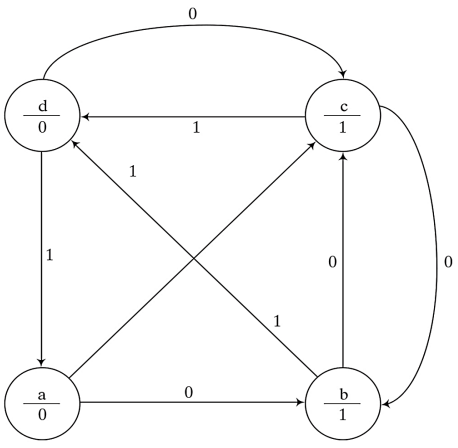
(a)



(b)

3. (20%) For the following two state diagrams, identify the Mealy Machine and Moore Machine, respectively. Prove or disprove that they are equivalent.





4. (10%) What is the difference between serial and parallel transfer? Explain how to convert serial data to parallel and parallel data to serial. What type of register is needed?
5. (15%) Design a modulo-9 counter using D FFs, with the counting sequence (0, 1, 2, 3, 4, 5, 6, 7, 8, 0, 1, ...), which produces $y = 1$ if the state '8' is encountered (i.e., when we go from state '8' to state '0'), and $y = 0$ otherwise. The counter stays in its current state iff $C = 0$, and makes state transition iff $C = 1$. You can use only D FFs. Show the state diagram and minimized state table, then derive the simplified output and excitation functions. Finally, show the schematic.
6. (15%) We are going to design a serial two's-complementor circuit using D FFs. A binary integer of arbitrary length is entered into the input X of the two's-complementor, with LSB first. When a given bit is entered on input X, the corresponding output bit is to appear during the same clock cycle on output Z. When the other input C becomes 1 for one clock cycle, it indicates that a sequence is complete and that the circuit is to be initialized to receive another sequence. Otherwise, C = 0. Give the state diagram and state table for the serial two's-complementor, and follow the design procedure step by step to obtain a circuit implemented by D FFs.

