EECS1010 Logic Design

Homework 5

Please work on the homework by yourself. Calculation/thinking process needs to be provided clearly. Submit your homework electronically on eeclass website.

Due date: 12/7 (Tue), 13:20.

1. (15%) Consider the timing diagram in Figure 1(a). D and Clock are the inputs to the circuits in Figure 1(b). Draw the waveforms of the Q_a, Q_b, and Q_c.

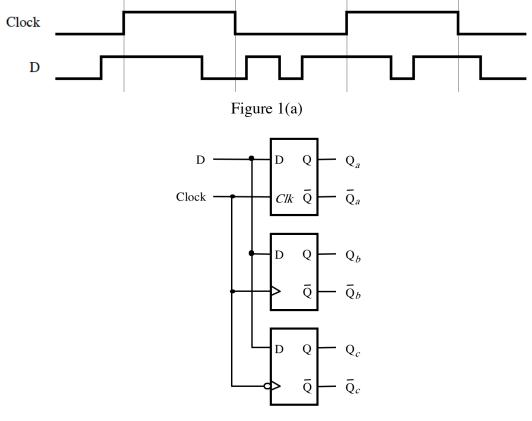


Figure 1(b)

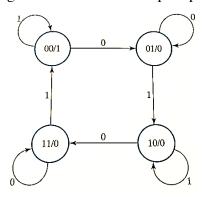
2. (15%) Reduce the number of states in the following state table and tabulate the reduced state table. Assume the initial state is A. Show the output sequence when the input sequence is 10100111001.

Present state	Next state		Output	
	x = 0	x = 1	x = 0	x = 1
A	F	В	0	0
В	D	Е	1	0
С	F	Е	0	0
D	G	A	1	0
Е	D	Е	1	0
F	F	В	1	1
G	G	A	1	0
Н	G	С	0	0

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3. (16%) Design a sequence detector that has one input w and one output z. The detector produces z = 1 when the previous two input values were 00 or 11; otherwise z = 0.

4. (16%) A sequential circuit has two flip-flops A and B, one input x and one output z. The state diagram is shown in the following figure. Design the circuit with D flip-flops using 1-hot state assignment.



5. (18%) A sequential circuit with two D flip-flops A and B, two inputs X and Y, and one output Z is specified by the following input equations:

$$D_A = X'B' + XY', D_B = A' + Y'B, Z = YA'B.$$

Draw the logic diagram, derive the state table and the state diagram of this circuit.

6. (20%) Derive the state table, state diagram, next-state equation, and output equation of the following figure.

