1. (15%) Consider the timing diagram in Figure 1(a). D and Clock are the inputs to the circuits in Figure 1(b). Draw the waveforms of the Q_a, Q_b, and Q_c.

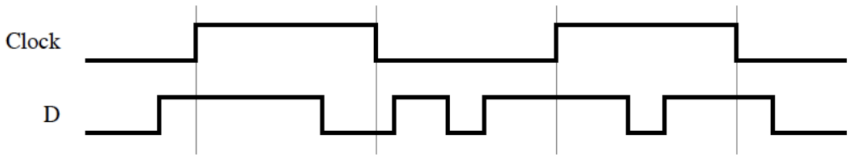


Figure 1(a)

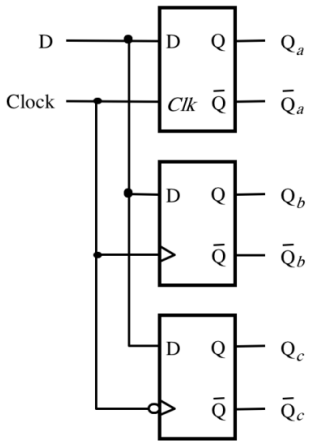
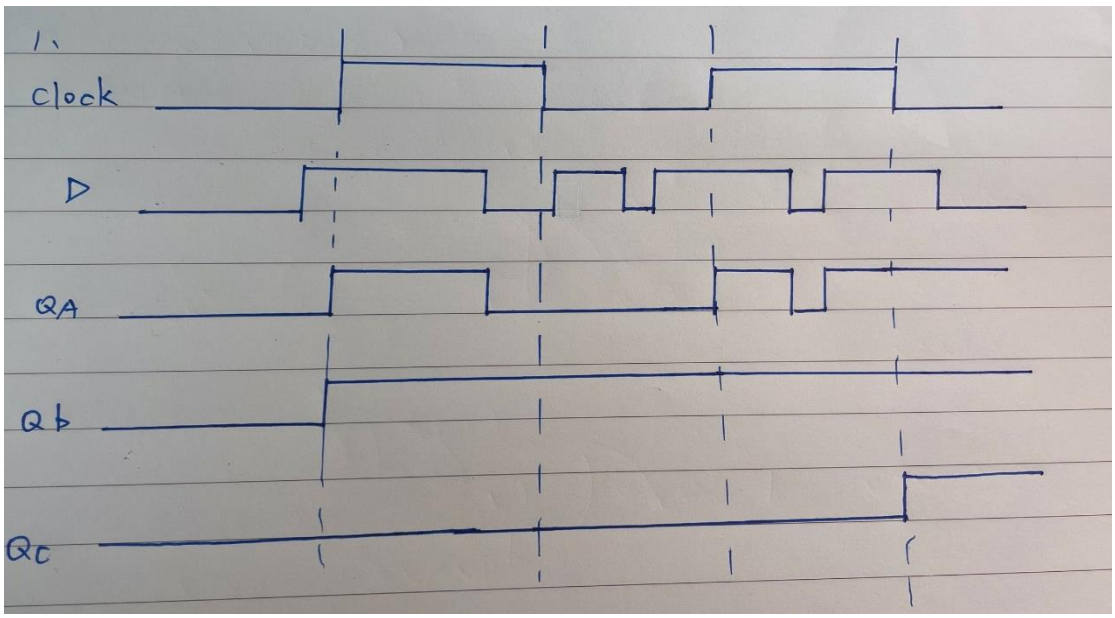


Figure 1(b)



2. (15%) Reduce the number of states in the following state table and tabulate the reduced state table. Show the output sequence when the input sequence is 10100111001.

Present state	Next state		Output	
	x = 0	x = 1	x = 0	x = 1
A	F	B	0	0
B	D	E	1	0
C	F	E	0	0
D	G	A	1	0
E	D	E	1	0
F	F	B	1	1
G	G	A	1	0
H	G	C	0	0

Present state	Next state		Output	
	x = 0	x = 1	x = 0	x = 1
A	F	B	0	0
B	D	~~E~~ B	1	0
~~C~~	~~F~~	~~E~~ B	~~0~~	~~0~~
D	~~G~~ D	A	1	0
~~E~~	~~D~~	~~E~~ B	~~1~~	~~0~~
F	F	B	1	1
~~G~~	~~G~~ D	~~A~~	~~1~~	~~0~~
H	~~G~~ D	~~C~~ A	0	0

Input : 10100111001

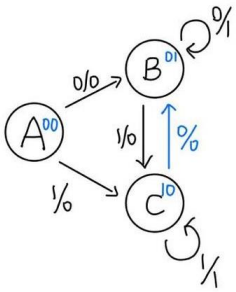
Initial state : A

State : A→B→D→A→F→F→B→B→B→D→D→A

Output : 01001100110

3. (16%) Design a sequence detector that has one input w and one output z. The detector produces z = 1 when the previous two input values were 00 or 11; otherwise z = 0.

A : initial state 00
B : "0" appear 01
C : "1" appear 10



present state w	present state x	input y	next state w^+	next state x^+	output z
0	0	0	0	1	0
0	0	1	1	0	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	0	1	0
1	0	1	1	0	1
1	1	0	X	X	X
1	1	1	X	X	X

w^+ : $w^+ = y$

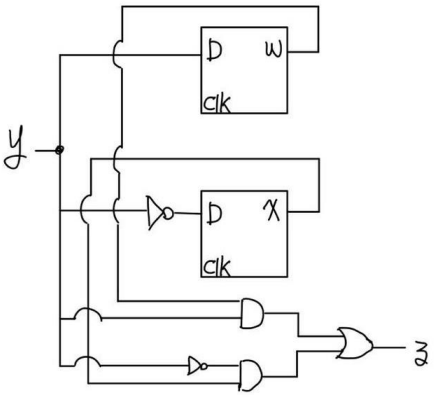
y \ wx	00	01	11	10
0	0	0	X	0
1	1	1	X	1

x^+ : $x^+ = y'$

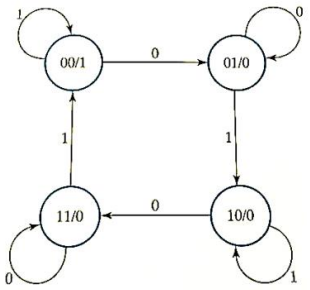
y \ wx	00	01	11	10
0	1	1	X	1
1	0	0	X	0

z : $z = xy' + wy$

y \ wx	00	01	11	10
0	0	1	X	0
1	0	0	X	1



4. (16%) A sequential circuit has two flip-flops A and B, one input x and one output z. The state diagram is shown in the following figure. Design the circuit with D flip-flops using 1-hot state assignment.



Truth table

	Y3	Y2	Y1	Y0	X	D3	D2	D1	D0	Z
1	0	0	0	0	0	x	x	x	x	x
2	0	0	0	1	0	0	0	1	0	1
3	0	0	1	0	0	0	0	1	0	0
4	0	0	1	1	0	x	x	x	x	x
5	0	1	0	0	0	1	0	0	0	0
6	0	1	0	1	0	x	x	x	x	x
7	0	1	1	0	0	x	x	x	x	x
8	0	1	1	1	0	x	x	x	x	x
9	1	0	0	0	0	1	0	0	0	0
10	1	0	0	1	0	x	x	x	x	x
11	1	0	1	0	0	x	x	x	x	x
12	1	0	1	1	0	x	x	x	x	x
13	1	1	0	0	0	x	x	x	x	x
14	1	1	0	1	0	x	x	x	x	x
15	1	1	1	0	0	x	x	x	x	x
16	1	1	1	1	0	x	x	x	x	x
17	0	0	0	0	1	x	x	x	x	x
18	0	0	0	1	1	0	0	0	1	1
19	0	0	1	0	1	0	1	0	0	0
20	0	0	1	1	1	x	x	x	x	x
21	0	1	0	0	1	0	1	0	0	0
22	0	1	0	1	1	x	x	x	x	x
23	0	1	1	0	1	x	x	x	x	x
24	0	1	1	1	1	x	x	x	x	x
25	1	0	0	0	1	0	0	0	1	0
26	1	0	0	1	1	x	x	x	x	x
27	1	0	1	0	1	x	x	x	x	x
28	1	0	1	1	1	x	x	x	x	x
29	1	1	0	0	1	x	x	x	x	x
30	1	1	0	1	1	x	x	x	x	x
31	1	1	1	0	1	x	x	x	x	x
32	1	1	1	1	1	x	x	x	x	x

KMAP

D0,x=0

Y3Y2 \ Y1Y0	00	01	11	10
00	x	0	x	0
01	0	x	x	x
11	x	x	x	x
10	0	x	x	x

D0,x=1

Y3Y2 \ Y1Y0	00	01	11	10
00	x	1	x	0
01	0	x	x	x
11	x	x	x	x
10	1	x	x	x

D1,x=0

Y3Y2 \ Y1Y0	00	01	11	10
00	x	1	x	1
01	0	x	x	x
11	x	x	x	x
10	0	x	x	x

D1,x=1

Y3Y2 \ Y1Y0	00	01	11	10
00	x	0	x	0
01	0	x	x	x
11	x	x	x	x
10	0	x	x	x

D2,x=0

Y3Y2 \ Y1Y0	00	01	11	10
00	x	0	x	0
01	0	x	x	x
11	x	x	x	x
10	0	x	x	x

D2,x=1

Y3Y2 \ Y1Y0	00	01	11	10
00	x	0	x	1
01	1	x	x	x
11	x	x	x	x
10	0	x	x	x

D3,x=0

Y3Y2 \ Y1Y0	00	01	11	10
00	x	0	x	0
01	1	x	x	x
11	x	x	x	x
10	1	x	x	x

D3,x=1

Y3Y2 \ Y1Y0	00	01	11	10
00	x	0	x	0
01	0	x	x	x
11	x	x	x	x
10	0	x	x	x

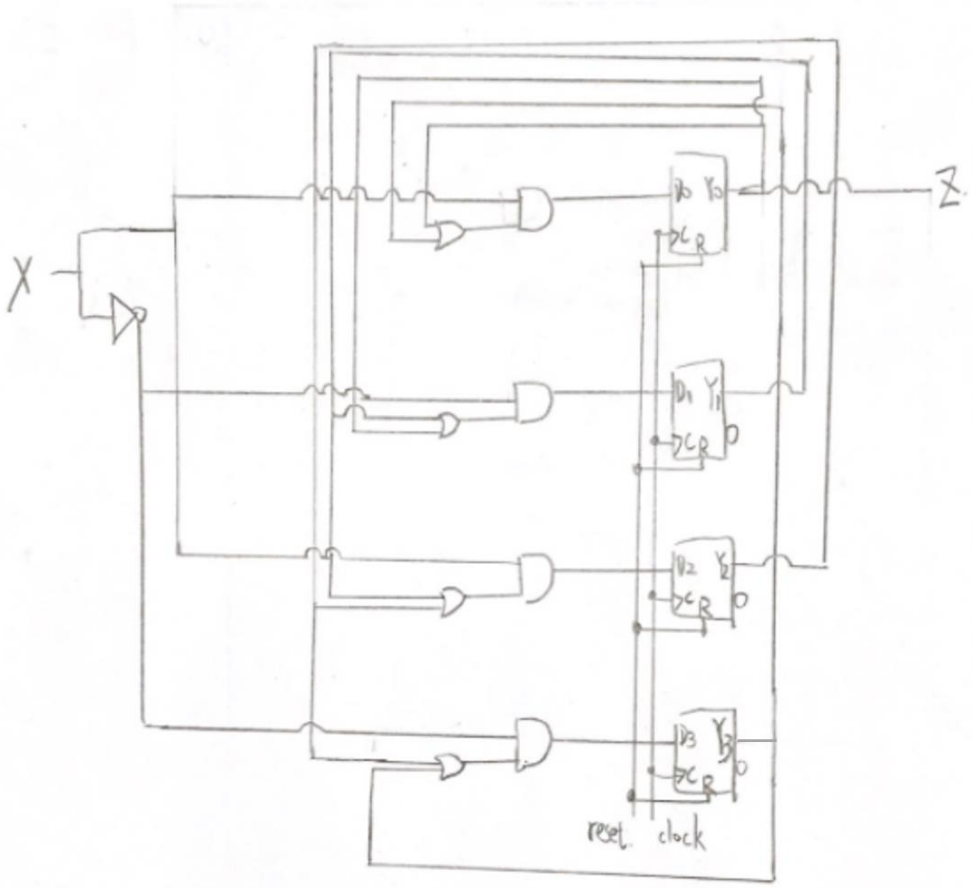
Z,x=0

Y3Y2 \ Y1Y0	00	01	11	10
00	x	1	x	0
01	0	x	x	x
11	x	x	x	x
10	0	x	x	x

Z,x=1

Y3Y2 \ Y1Y0	00	01	11	10
00	x	1	x	0
01	0	x	x	x
11	x	x	x	x
10	0	x	x	x

$$D_0 = X(Y_0 + Y_3)$$
$$D_1 = \overline{X}(Y_0 + Y_1)$$
$$D_2 = X(Y_1 + Y_2)$$
$$D_3 = \overline{X}(Y_2 + Y_3)$$
$$Z = Y_0$$

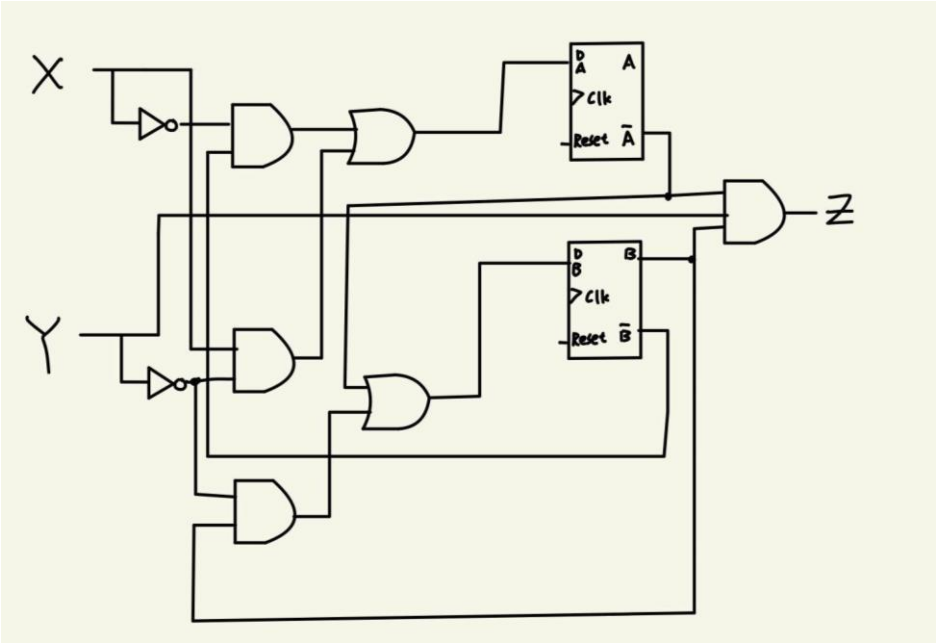

X
Z
reset
clock

5. (18%) A sequential circuit with two *D* flip-flops A and B, two inputs *X* and *Y*, and one output Z is specified by the following input equations:

D_A=X'B'+XY', D_B=A'+Y'B, Z=YA'B.

Draw the logic diagram, derive the state table and the state diagram of this circuit.

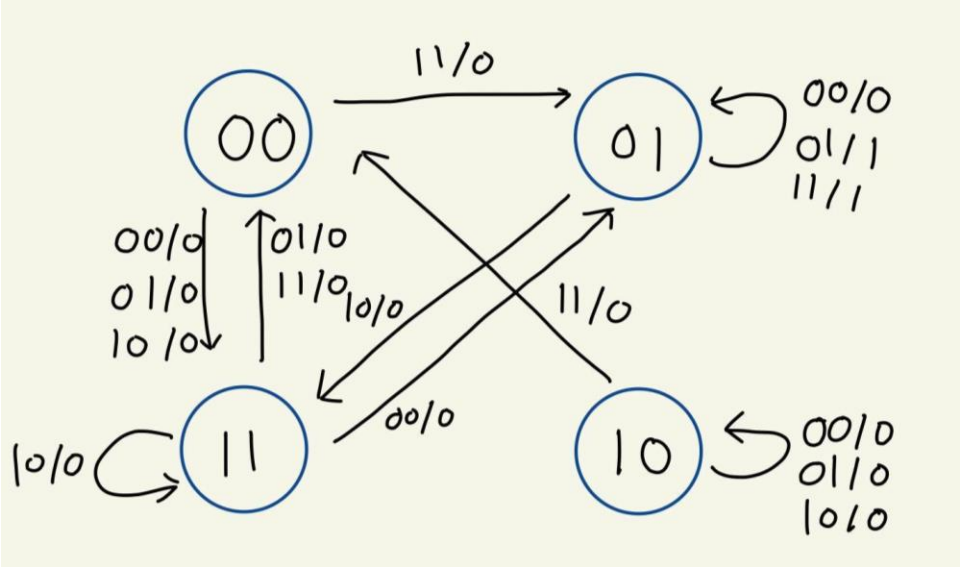
Logic diagram:



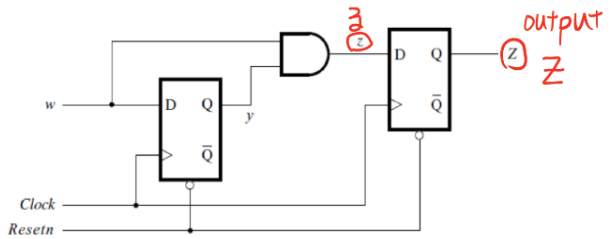
State table:

Current state		input		Next state		output
A	B	X	Y	A+1	B+1	Z
0	0	0	0	1	1	0
0	0	0	1	1	1	0
0	0	1	0	1	1	0
0	0	1	1	0	1	0
0	1	0	0	0	1	0
0	1	0	1	0	1	1
0	1	1	0	1	1	0
0	1	1	1	0	1	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	1	0	0
1	0	1	1	0	0	0
1	1	0	0	0	1	0
1	1	0	1	0	0	0
1	1	1	0	1	1	0
1	1	1	1	0	0	0

State diagram:



6. (20%) Derive the state table, state diagram, next-state equation, and output equation of the following figure.



① State table :

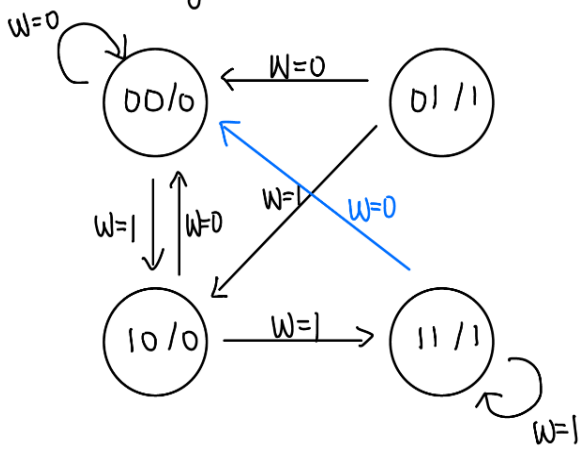
$Z = wy$

$y(t+1) = w$

$Z(t+1) = Z$
$= wy$

Present state		Next state				Output
		w=0		w=1		
y	Z	y	Z	y	Z	Z
0	0	0	0	1	0	0
0	1	0	0	1	0	1
1	1	0	0	1	1	1
1	0	0	0	1	1	0

② State diagram :



③ Next state / Output equation

$y(t+1) = w$

$Z(t+1) = wy$

$Z_{,out} = Z$