1. (20%) A sequential circuit with two *D* flip-flops A and B, two inputs *x* and *y*, and one output z is specified by the following next state equations and output equation: **(林致佑)**

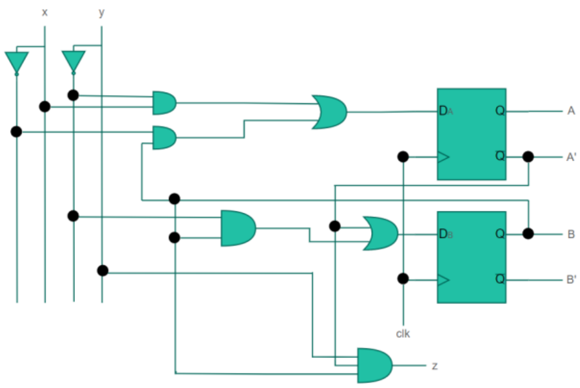
A(t+1)=x'B(t)+xy', B(t+1)=A'(t)+y'B(t), z=yA'B

(a) Draw the logic diagram of the circuit.

(b) Derive the state table.

(c) Derive the state diagram.

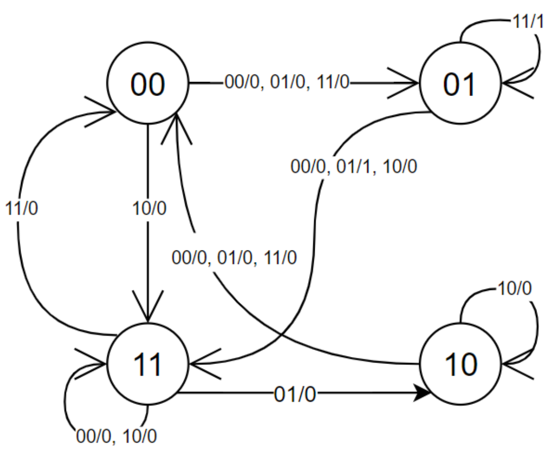
(a) logic diagram:



(b) state table:

A(t)	B(t)	x	y	A(t+1)	B(t+1)	z
0	0	0	0	0	1	0
0	0	0	1	0	1	0
0	0	1	0	1	1	0
0	0	1	1	0	1	0
0	1	0	0	1	1	0
0	1	0	1	1	1	1
0	1	1	0	1	1	0
0	1	1	1	0	1	1
1	0	0	0	0	0	0
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	0	1	1	0	0	0
1	1	0	0	1	1	0
1	1	0	1	1	0	0
1	1	1	0	1	1	0
1	1	1	1	0	0	0

(c) state diagram:



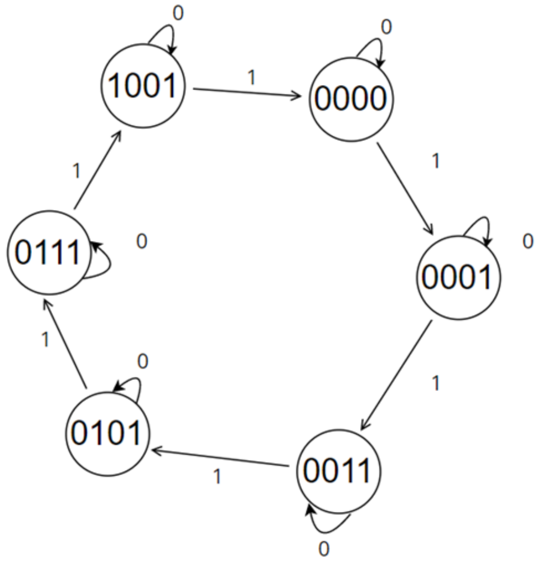
2. (20%) Design a synchronous finite state machine whose output is the sequence 0, 1, 3, 5, 7, 9, 0, 1, 3, 5, 7, 9, 0, ... The machine is controlled by a single input, ***Run***, so that counting occurs while ***Run*** is 1, suspends while ***Run*** is 0, and resumes the count when ***Run*** is 1 again. Clearly state any assumptions that you make.

(陳冠霖)

Follow the design procedure:

1) Only one input Run; we may try to use the states to be the outputs (A3A2A1A0).

2) Determine the states. The states are the outputs.



3) 4) 5) Derive the next state table

	Input	Present state				Next State			
	Run	A3(t)	A2(t)	A1(t)	A0(t)	A3(t+1)	A2(t+1)	A1(t+1)	A0(t+1)
0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0	0	1
2	0	0	0	1	0	x	x	x	x
3	0	0	0	1	1	0	0	1	1
4	0	0	1	0	0	x	x	x	x
5	0	0	1	0	1	0	1	0	1
6	0	0	1	1	0	x	x	x	x
7	0	0	1	1	1	0	1	1	1
8	0	1	0	0	0	x	x	x	x
9	0	1	0	0	1	1	0	0	1
10	0	1	0	1	0	x	x	x	x
11	0	1	0	1	1	x	x	x	x
12	0	1	1	0	0	x	x	x	x

13	0	1	1	0	1	x	x	x	x
14	0	1	1	1	0	x	x	x	x
15	0	1	1	1	1	x	x	x	x
16	1	0	0	0	0	0	0	0	1
17	1	0	0	0	1	0	0	1	1
18	1	0	0	1	0	x	x	x	x
19	1	0	0	1	1	0	1	0	1
20	1	0	1	0	0	x	x	x	x
21	1	0	1	0	1	0	1	1	1
22	1	0	1	1	0	x	x	x	x
23	1	0	1	1	1	1	0	0	1
24	1	1	0	0	0	x	x	x	x
25	1	1	0	0	1	0	0	0	0
26	1	1	0	1	0	x	x	x	x
27	1	1	0	1	1	x	x	x	x
28	1	1	1	0	0	x	x	x	x
29	1	1	1	0	1	x	x	x	x
30	1	1	1	1	0	x	x	x	x
31	1	1	1	1	1	x	x	x	x

6)

$$A3(t+1) = D_{A3}\big(Run, A3(t), A2(t), A1(t), A0(t)\big) = \sum(9,23)$$

$$A2(t+1) = D_{A2}\big(Run, A3(t), A2(t), A1(t), A0(t)\big) = \sum(5,7,19,21)$$

$$A1(t+1) = D_{A1}\big(RunA3(t), A2(t), A1(t), A0(t)\big) = \sum(3,7,17,21)$$

$$A0(t+1) = D_{A0}\big(Run, A3(t), A2(t), A1(t), A0(t)\big) = \sum(1,3,5,7,9,16,17,19,21,23)$$

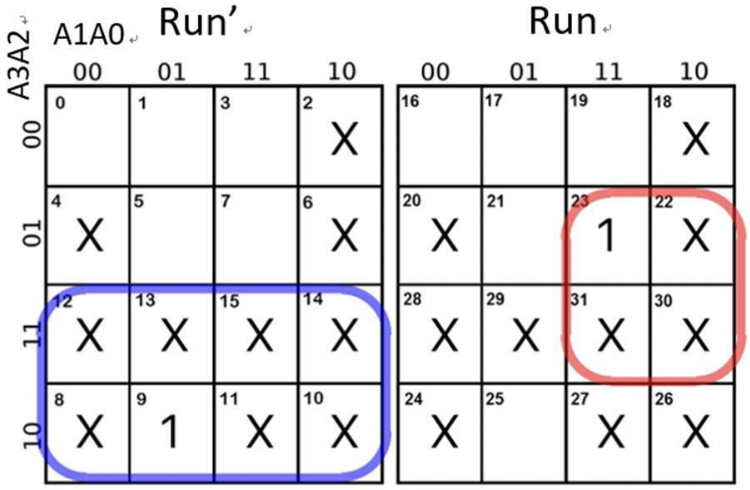
All equations at above have the same don't-care condition,

d=Σ (2, 4, 6, 8, 10~15, 18, 20, 22, 24, 26~31).

7) Choose D FFs (default).

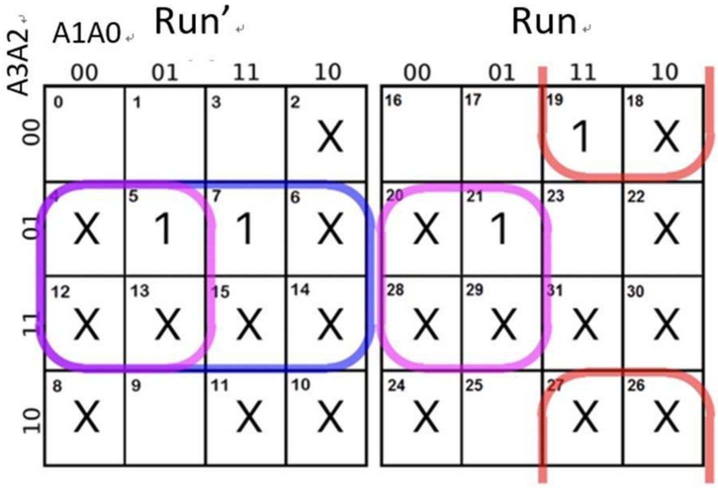
8)

For D_{A3}



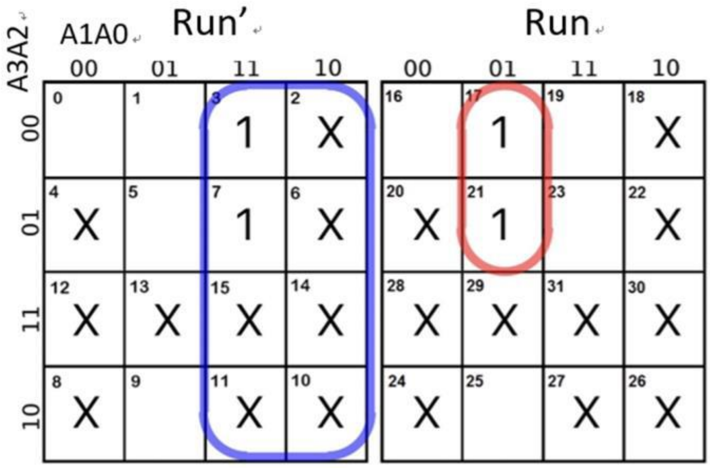
D_{A3} = Run(A2A1) + Run’(A3)

For D_{A2}



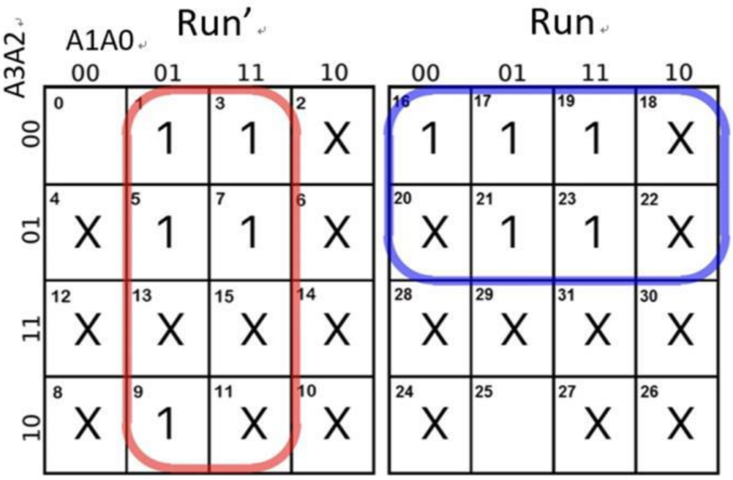
D_{A2} = Run(A2’A1) + Run’(A2) + A2A1’

For D_{A1}



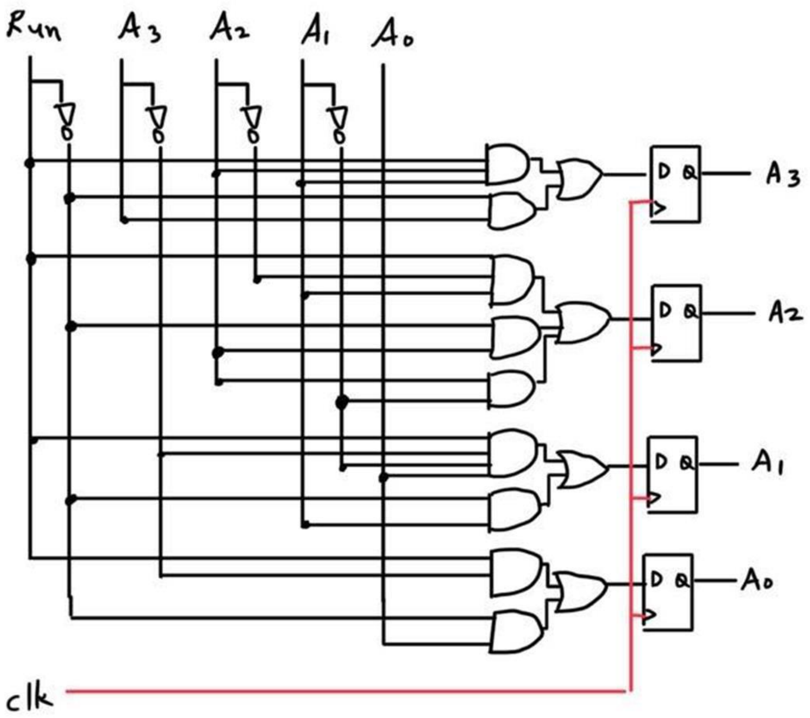
D_{A1} = Run(A3'A1'A0) + Run'(A1)

For D_{A0}



D_{A0} = Run(A3') + Run'(A0)

9)



3. (20%) For the state table below:

(a) Reduce the number of states in the following state table and tabulate the reduced state table. Assume the initial state is A.

(b) Draw the state diagram using the reduced state table.

(c) Draw the logic diagram of the logic.

(d) Show the output sequence when the input sequence is 111010101.

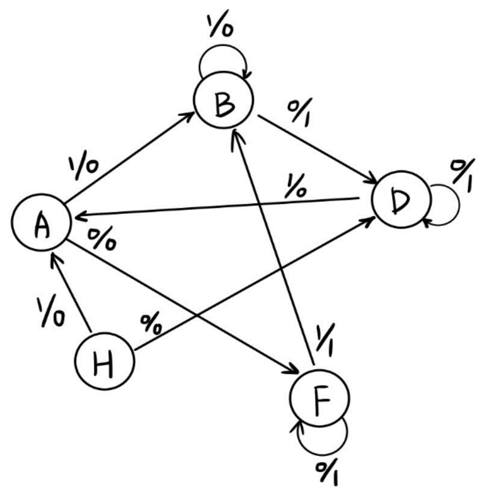
(呂易緯)

Present state	Next state		Output	
	x = 0	x = 1	x = 0	x = 1
A	F	B	0	0
B	D	E	1	0
C	F	E	0	0
D	G	A	1	0
E	D	E	1	0
F	F	B	1	1
G	G	A	1	0
H	G	C	0	0

(a)

Present state	Next state		Output	
	x = 0	x = 1	x = 0	x = 1
A	F	B	0	0
B	D	~~E~~ B	1	0
~~C~~	~~F~~	~~E~~ B	~~0~~	~~0~~
D	~~G~~ D	A	1	0
~~E~~	~~D~~	~~E~~ B	~~1~~	~~0~~
F	F	B	1	1
~~G~~	~~G~~ D	~~A~~	~~1~~	~~0~~
H	~~G~~ D	~~C~~ A	0	0

(b)



(c)

Present State				Input	Next State				Output
	A(t)	B(t)	C(t)	x		A(t+1)	B(t+1)	C(t+1)	y
A	0	0	0	**0**	**F**	0	1	1	**0**
	0	0	0	**1**	**B**	0	0	1	**0**
B	0	0	1	**0**	**D**	0	1	0	**1**
	0	0	1	**1**	**B**	0	0	1	**0**
D	0	1	0	**0**	**D**	0	1	0	**1**
	0	1	0	**1**	**A**	0	0	0	**0**
F	0	1	1	**0**	**F**	0	1	1	**1**
	0	1	1	**1**	**B**	0	0	1	**1**
H	1	0	0	**0**	**D**	0	1	0	**0**
	1	0	0	**1**	**A**	0	0	0	**0**

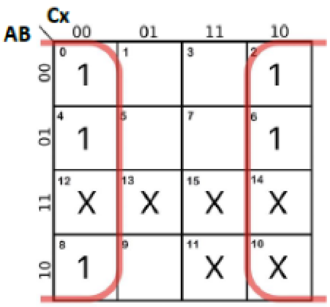
Next state equations

$B(t+1) = D_B(A(t), B(t), C(t), x) = \Sigma(0,2,4,6,8)$, $d = \Sigma(10,11,12,13,14,15)$

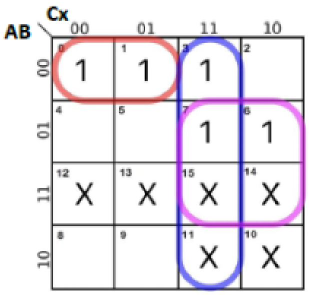
$C(t+1) = D_C(A(t), B(t), C(t), x) = \Sigma(0,1,3,6,7)$, $d = \Sigma(10,11,12,13,14,15)$

Output equation

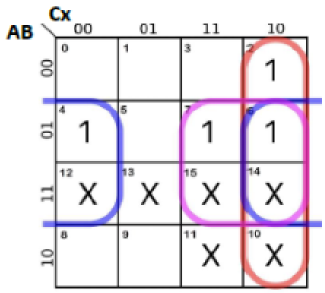
$y(A(t), B(t), C(t), x) = \Sigma(2,4,6,7)$, $d = \Sigma(10,11,12,13,14,15)$



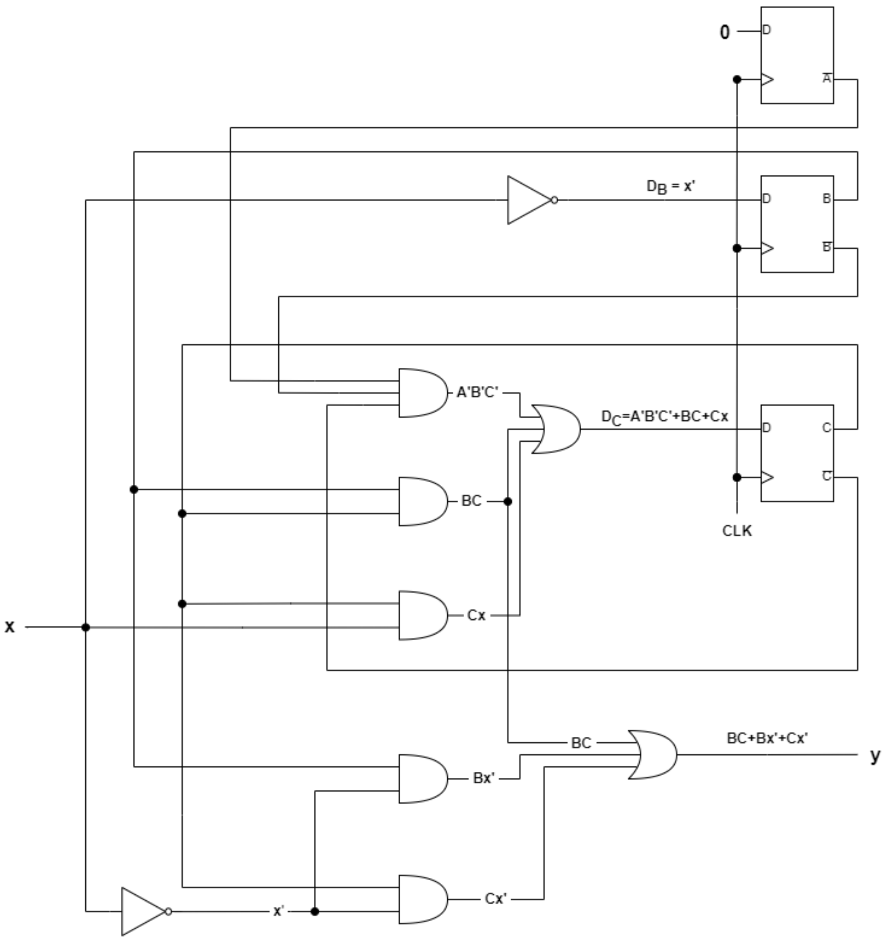
$D_B = x'$



$D_C = A'B'C' + BC + Cx$



$y = BC + Bx' + Cx'$



(d)

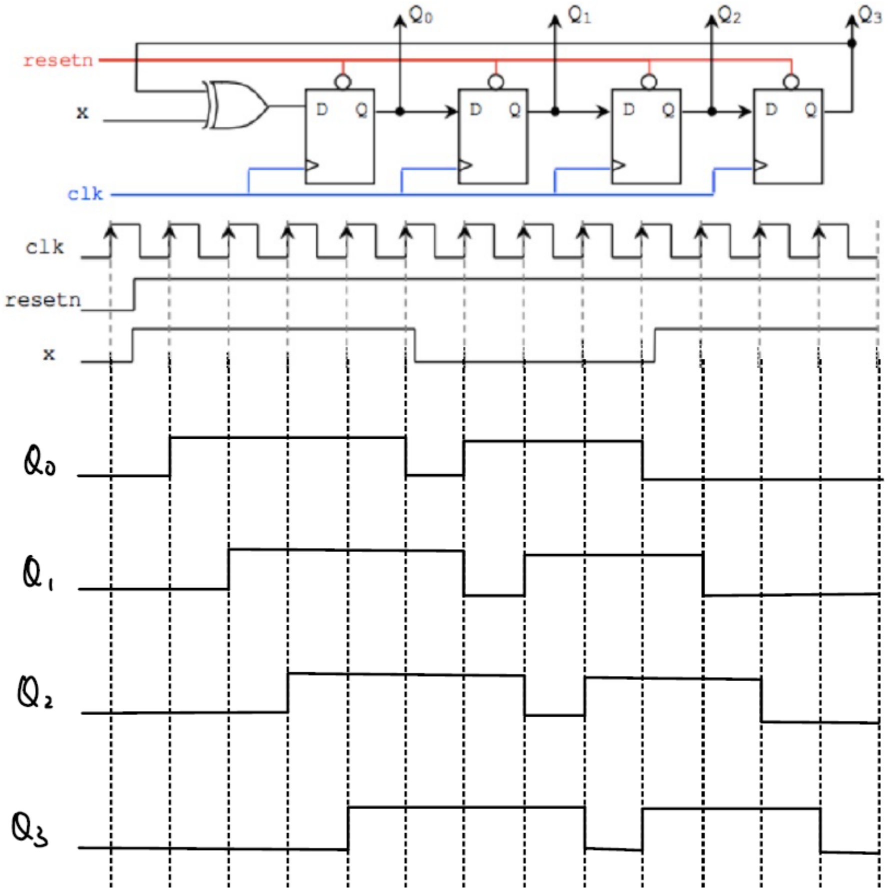
Input : 111010101

Initial State : A

State : A → B → B →B → D → A → F → B → D → A

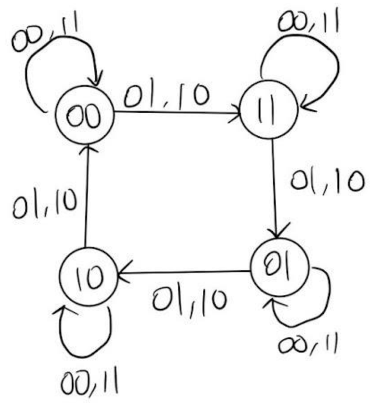
Output : 000100110

4. (20%) Derive the timing diagram of the following circuit. Draw Q_3, Q_2, Q_1, and Q_0. **(林彥岑)**



5. (20%) Design a sequential circuit with two *D* flip-flops *A* and *B* and two inputs *X* and *Y*. When $X = Y$, the state of the circuit remains the same. When $X \neq Y$, the circuit goes through the state transitions from 00 to 11 to 01 to 10, back to 00, and then repeats. **(徐浩庭)**

State diagram



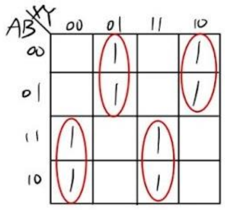
State table

Present state A	Present state B	Next state X=Y (00 or 11)	Next state X≠Y (01 or 10)
0	0	0 0	1 1
1	1	1 1	0 1
0	1	0 1	1 0
1	0	1 0	0 0

Truth table

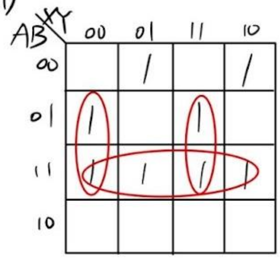
A(t)	B(t)	X	Y	A(t+1)	B(t+1)
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	1	1
0	0	1	1	0	0
0	1	0	0	0	1
0	1	0	1	1	0
0	1	1	0	1	0
0	1	1	1	0	1
1	0	0	0	1	0
1	0	0	1	0	0
1	0	1	0	0	0
1	0	1	1	1	0
1	1	0	0	1	1
1	1	0	1	0	1
1	1	1	0	0	1
1	1	1	1	1	1

A(t+1)



$D_A = AX'Y' + A'X'Y + AXY + A'XY'$

B(t+1)



$D_B = BX'Y' + BXY + AB + A'B'X'Y + A'B'XY'$

Logic Diagram