1. (30%) Design a 4-bit two parameter comparator (input A and B, A:$a_3a_2a_1a_0$, B:$b_3b_2b_1b_0$ are both in 2's complement representation) and output the smaller one S($s_3s_2s_1s_0$).

(賴聖耘)

先用 comparator，當(A<B)時，輸出 1，若是(A>=B)，則輸出 0。

再使用 MUX，以 comparator 的輸出作為 select，

當 select==1(A<B)時，輸出 A3A2A1A0，

當 select==0(A>=B)時，輸出 B3B2B1B0。

By algorithm to build a regular circuit

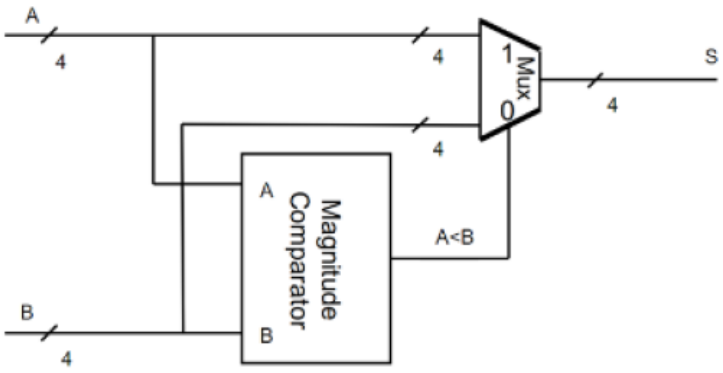
$$A=A_3A_2A_1A_0,\ B=B_3B_2B_1B_0$$

因為是 2's-complement ，MSB 為 0 代表正數，MSB 為 1 代表負數，且因為規定是 A,B 都是 4-bit，所以 MSB 也會因 sign extension 而補上 1 或是 0。在判斷大小時，就可以使用 A3B3'，其他位置則是使用課本上的 bit equality。

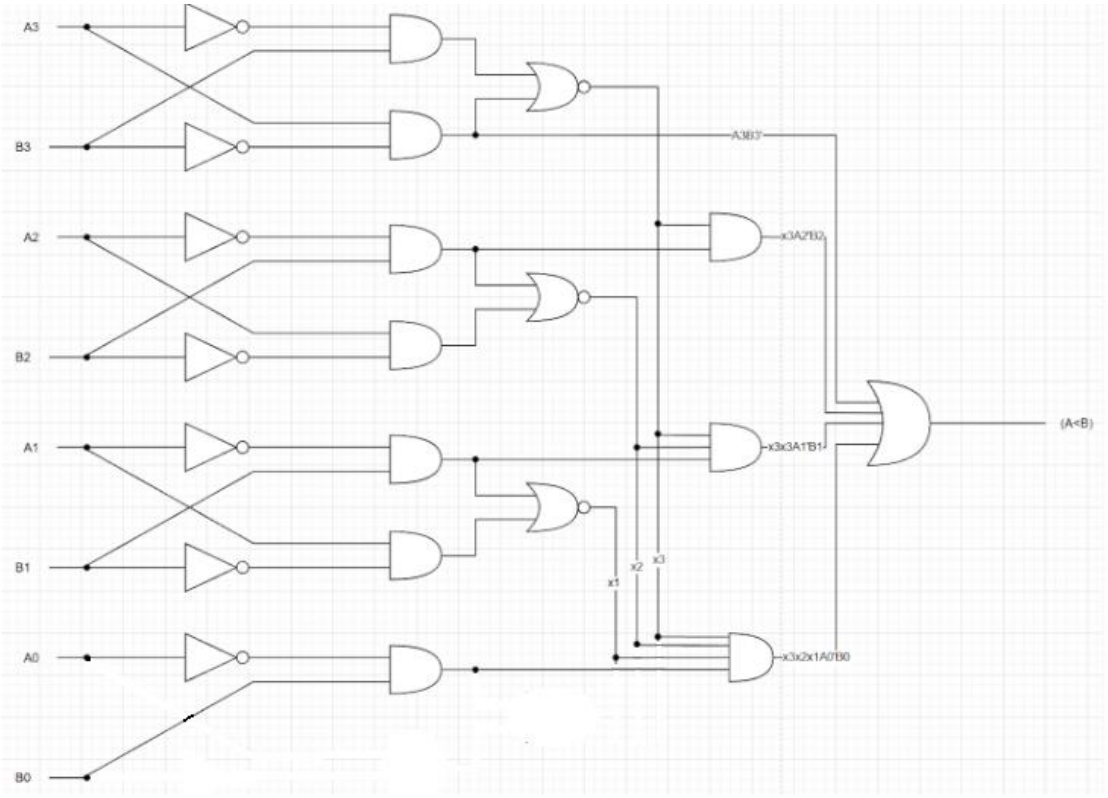
$$\text{equality } x_i=A_iB_i+A_i'B_i'$$

$$(A<B)=A_3B_3'+x_3A_2'B_2+x_3x_2A_1'B_1+x_3x_2x_1A_0'B_0$$

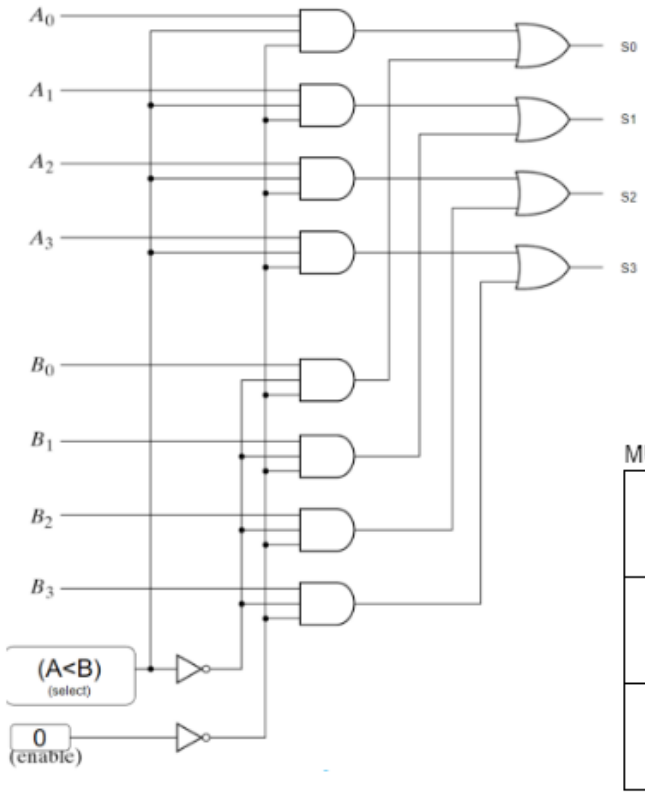
Block diagram:



4-bit comparator logic diagram:



4-bit 2:1 MUX logic diagram:



MUX function table:

E(enable)	A<B(select)	Output
0	0	Select B
0	1	Select A

2. (10%) Construct a 5-to-32-line decoder with four 3-to-8-line decoders with enable and a 2-to-4-line decoder.

(陳冠霖)

inputs: A0 to A4

outputs: D0 to D31

Since we have four 3-to-8-lines decoders with enable, we may consider deriving enable signals from part of our inputs; with the 2-to-4-line decoder, we obtain E0 to E3 and use them as enable signals to the four 3-to-8-line decoders.