EECS1010 Logic Design

## HW4-2

1. (30%) Design a 4-bit two parameter comparator (input A and B, A: $a_3a_2a_1a_0$ , B: $b_3b_2b_1b_0$  are both in 2's complement representation) and output the smaller one  $S(s_3s_2s_1s_0)$ .

2. (10%) Construct a 5-to-32-line decoder with four 3-to-8-line decoders with enable and a 2-to-4-line decoder.