HW7

1. A sequential circuit with two *D* flip-flops A and B, two inputs *X* and *Y*, and one output Z is specified by the following input equations:

   D_A=XA'+X'Y, D_B=B'+Y'A, Z=Y'AB'

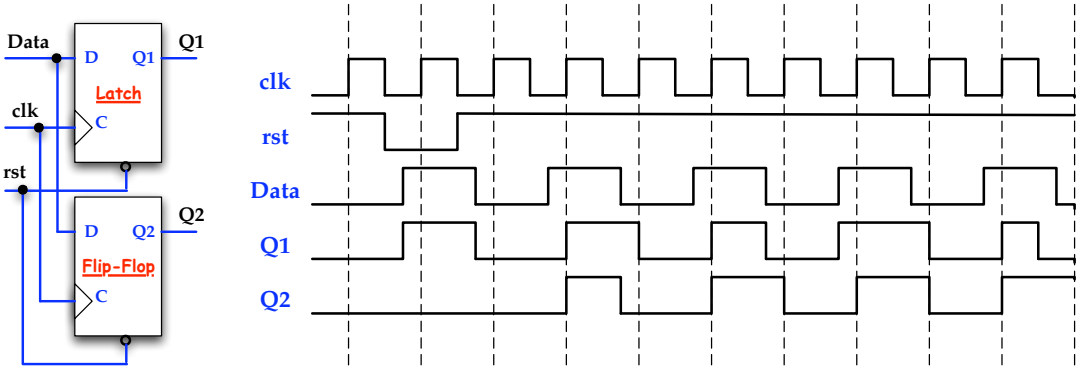
   (a) Draw the logic diagram of the circuit.

   (b) Derive the state table.

   (c) Derive the state diagram.

2. Design a sequential circuit with two *D* flip-flops *A* and *B* and one input *X*. When *X* = 0, the state of the circuit remains the same. When *X* = 1, the circuit goes through the state transitions from 00 to 10 to 11 to 01, back to 00, and then repeats.

3. For the D-type positive edge-triggered flip-flop and D-type positive level-sensitive (level-triggered) latch with the same clock (clk), asynchronous reset signal (rst), and input (Data) below. Assume the initial state of both the flip-flop and latch are '0', and both devices are with 0 D-to-Q delay. Point out the incorrect parts for Q1 and Q2 in the timing diagram and redraw the correct timing diagram.



4. A sequential circuit has two flip-flops A and B, one input X, and one output Y. The state diagram is shown in Figure 5-44. Design the circuit with D flip-flops using a 1-hot state assignment.

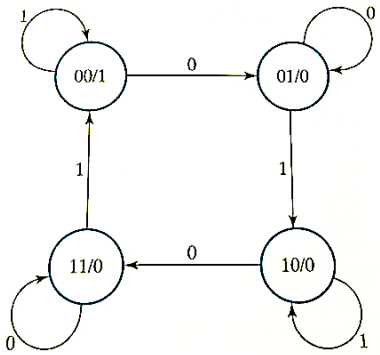


FIGURE 5-44
State Diagram for Problem 5–26

5. Draw the state diagram of the sequential circuit specified by the following state table.

Present State		Inputs		Next State		Output
A	B	X	Y	A	B	Z
0	0	0	0	0	0	0
0	0	0	1	0	1	0
0	0	1	0	1	0	1
0	0	1	1	1	1	1
0	1	0	0	0	1	1
0	1	0	1	1	0	1
0	1	1	0	1	0	0
0	1	1	1	0	0	0
1	0	0	0	1	1	1
1	0	0	1	1	1	0
1	0	1	0	1	1	1
1	0	1	1	1	0	0
1	1	0	0	0	0	0
1	1	0	1	0	0	1
1	1	1	0	0	0	0
1	1	1	1	0	1	1

6. Design a recognizer that recognizes an input sequence that has at least three 1's. The recognizer has a single input X, and a single output Y, and one asynchronous Reset input signal. The recognizer sets the output Y to 1 if the input signal X was equal to 1 in at least 3 clock cycles after reset. (a) Derive the state diagram. (b) Encode the states to minimize the combinational logic. (c) Draw the logic diagram using D flip-flops.

7. Use Verilog to verify the function in Prob. 2 with simulation results.

8. Reduce the number of states in the following state table and tabulate the reduced state table.

Present State	Next State		Output	
	x=0	x=1	x=0	x=1
a	f	b	0	0
b	d	e	1	0
c	f	e	0	0
d	g	a	1	0
e	d	e	1	0
f	f	b	1	1
g	g	a	1	0
h	g	c	0	0

Show that the same output sequences are obtained for both the state table of the previous problem and the reduced state table from the previous problem. The state-circuit starts from state a, and the input sequence is 10110101001.