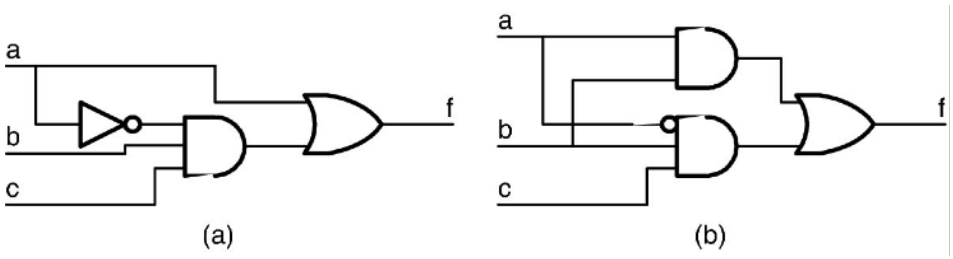
HW4

1. Majority Indicator: Design a voting machine for three people. When there is more than one person agree on some case (with input 1), the case will be passed (with output 1); otherwise, the case will be rejected (with output 0). (10%)
   (a) Derive the truth table.
   (b) Derive the simplified Boolean expressions for A, B, and C using maps in sum-of-products and product-of-sum forms, respectively.
   (c) Draw the related logic diagram.

2. Fix the hazard that may occur in the following figures: (10%)



3. Design a combinational circuit with three inputs, x (MSB),y, and z (LSB), and three outputs, A (MSB), B, and C (LSB). When the binary input is 0, 1, or 2, the binary output is three greater than the input (xyz=001 (1) => ABC=100 (4), xyz=010 (2) => ABC=101 (5).). When the binary input is 3, 4, 5, 6, or 7, the binary is two less than the input (xyz=110(6) => ABC=100 (4), xyz=100 (4) => ABC=010(2)). (10%)
   (a) Derive the truth table.
   (b) Derive the simplified Boolean expressions for A, B, and C using maps.
   (c) Draw the related logic diagram.

4. Design an excess-3-to-binary decoder using the unused combinations of the code as don't-care conditions. (10%)

5. Simplify the following Boolean expressions to a minimum number of literals, and implement with two-level NAND-NAND and NOR-NOR gates, respectively. (10%)
   (a) xy'z+xy'z'+xyz',
   (b) (y'z+xw')(xw+y'z).

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6. Simplify the following expression. Do not use k-map but use cube method. (10%)

$$F(A, B, C, D, E) = \sum(0, 2, 4, 6, 9, 13, 21, 23, 25, 29, 31)$$

7. A half adder is a circuit that takes in one-bit binary numbers a and b, and outputs a sum s and a carry out co. The concatenation of xo and s, is the two-bit value that results from adding a and b (e.g. if a=1, b=1, s=0, and co=1). (10%)
   (a) Derive the truth table of a half adder.
   (b) Derive the Boolean expression of co and s in the simplest sum-of-product form.
   (c) Find the prime implicants and essential prime implicants of co and s.

8. Use Verilog to simulate the half adder in problem 7. (10%)

9. Use Verilog to simulate the majority detector in problem 1. (10%)

10. Which of the following circuits are combinational? Each box in the figure is itself a combinational circuits. (10%)