2016 Logic Design HW8

8.1

Shift 1: 01011

Shift 2: 10110

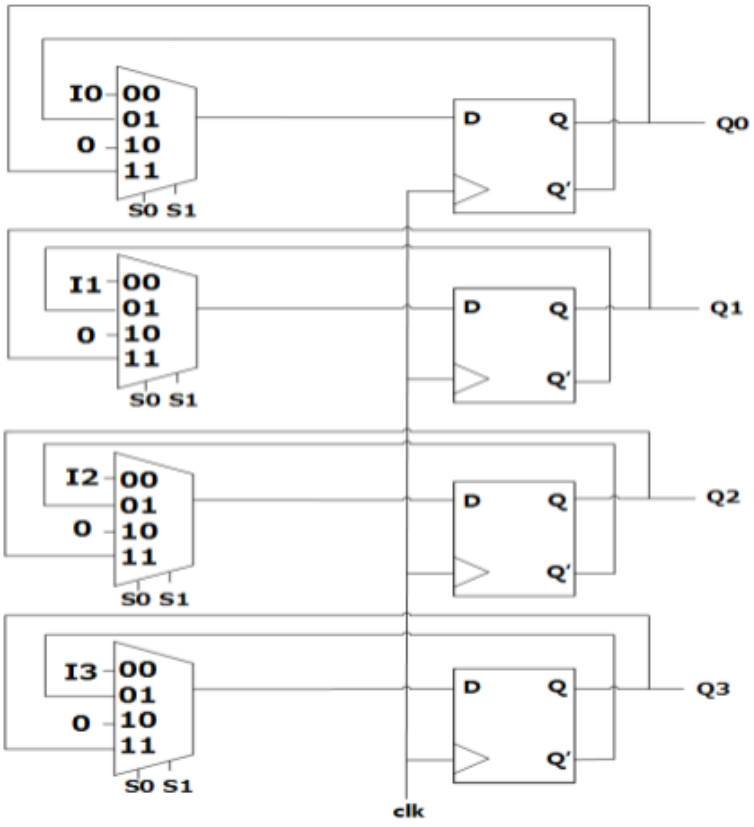
Shift 3: 01101

Shift 4: 11010

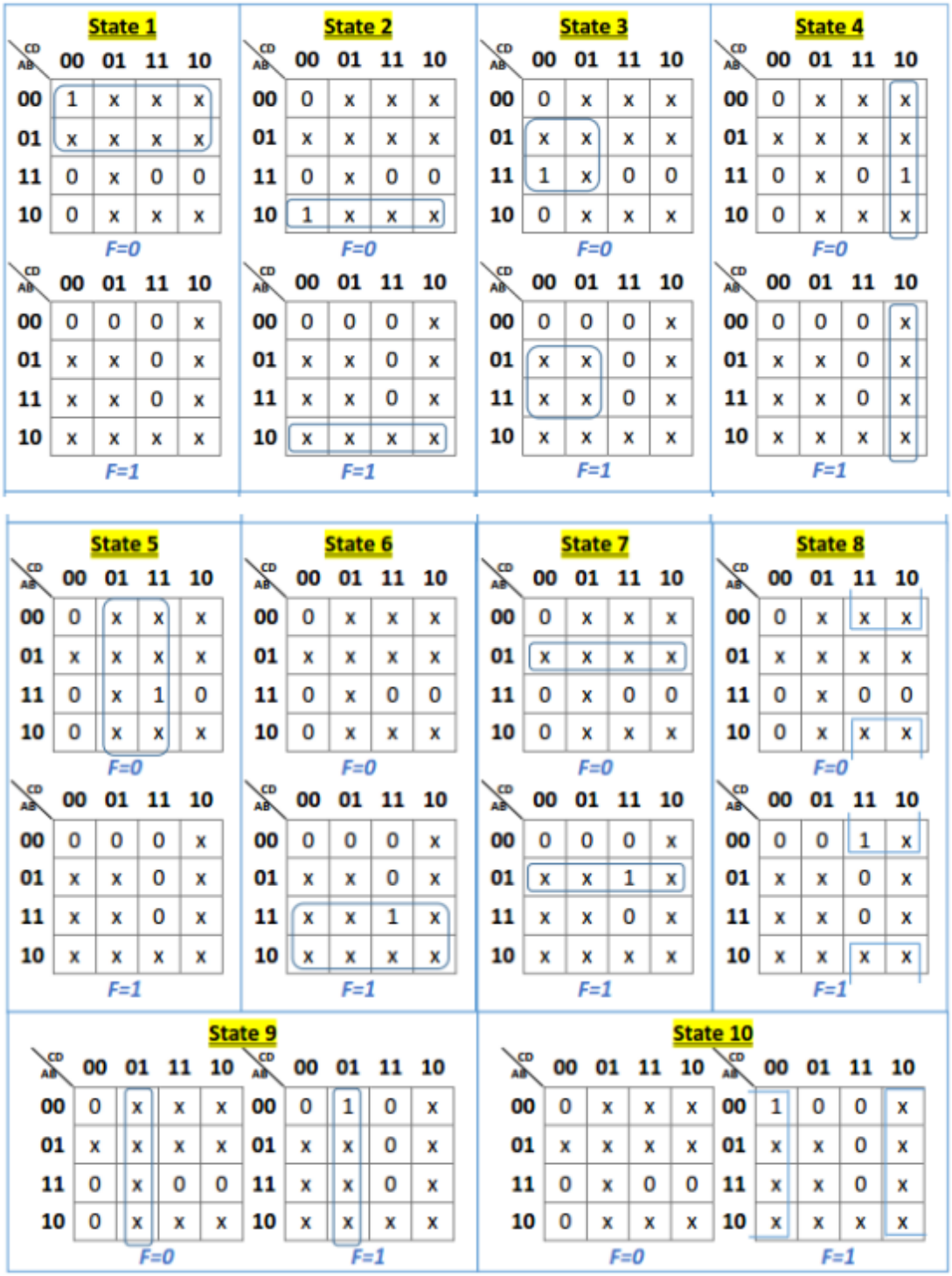
Shift 5: 10101

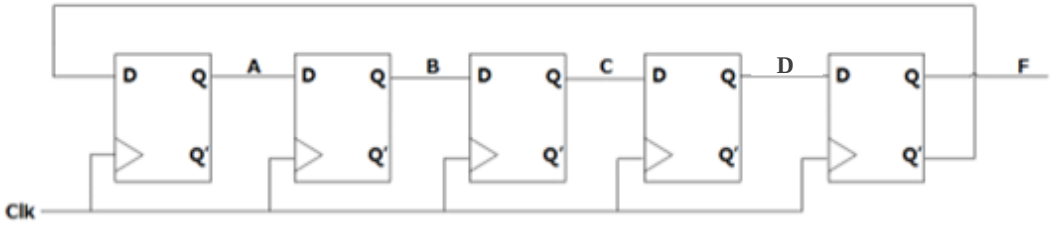
8.2

2.



8.3


State 1
State 2
State 3
State 4
State 5
State 6
State 7
State 8
State 9
State 10
CD
AB
00 01 11 10
F=0
F=1



Sequence Number	A	B	C	D	F	AND gate for output
1	0	0	0	0	0	A'F'
2	1	0	0	0	0	AB'
3	1	1	0	0	0	BC'
4	1	1	1	0	0	CD'
5	1	1	1	1	0	DF'
6	1	1	1	1	1	AF
7	0	1	1	1	1	A'B
8	0	0	1	1	1	B'C
9	0	0	0	1	1	C'D
10	0	0	0	0	1	D'F

8.4

(a)1,4,7

A	B	C	D_A	D_B	D_C
0	0	0	X	X	X
0	0	1	1	0	0
0	1	0	X	X	X
0	1	1	X	X	X
1	0	0	1	1	1
1	0	1	X	X	X
1	1	0	X	X	X
1	1	1	0	0	1

D_A:

A \ BC	00	01	11	10
0	X	1	X	X
1	1	X	0	X

$D_A=B'$

D_B:

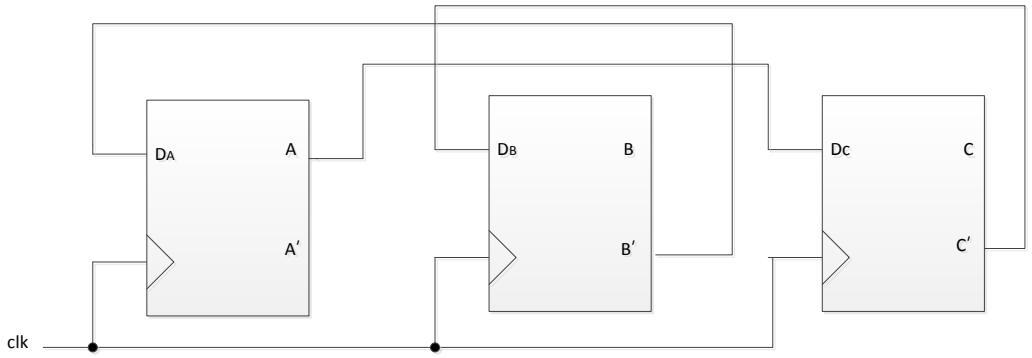
A \ BC	00	01	11	10
0	X	0	X	X
1	1	X	0	X

$D_B=C'$

D_C:

A \ BC	00	01	11	10
0	X	0	X	X
1	1	X	1	X

$D_C=A$



(b)0,2,4,6,7

A	B	C	D_A	D_B	D_C
0	0	0	0	1	0
0	0	1	X	X	X
0	1	0	1	0	0
0	1	1	X	X	X
1	0	0	1	1	0
1	0	1	X	X	X
1	1	0	1	1	1
1	1	1	0	0	0

D_A:

A \ BC	00	01	11	10
0	0	X	X	1
1	1	X	0	1

$D_A=BC'+AC'$

D_B:

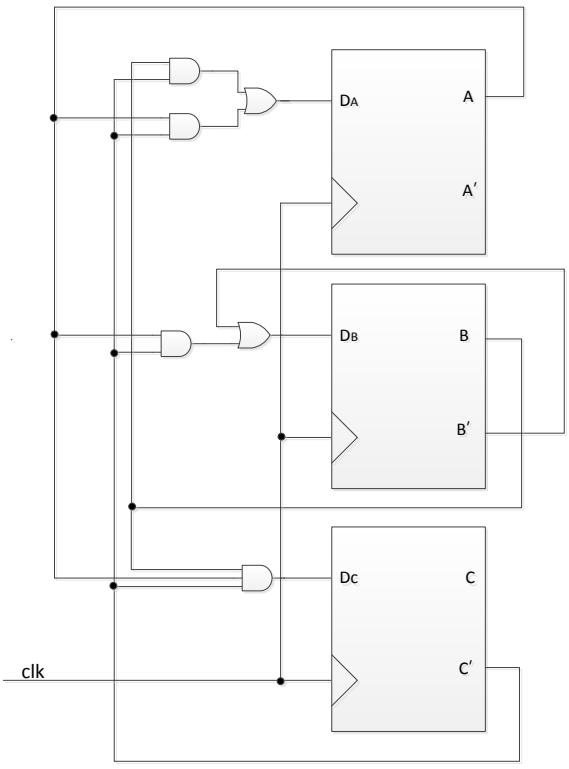
A \ BC	00	01	11	10
0	1	X	X	0
1	1	X	0	1

$D_B=B'+AC'$

D_C:

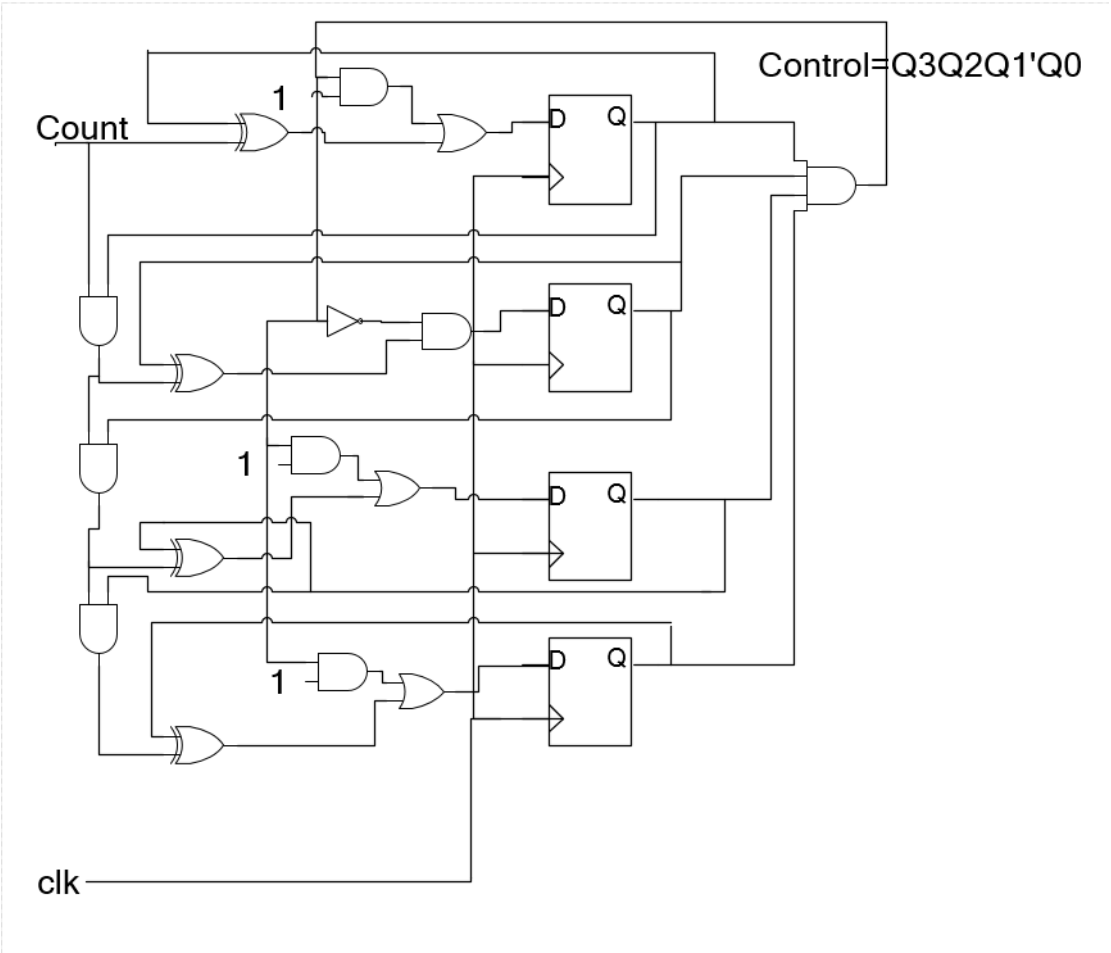
A \ BC	00	01	11	10
0	0	X	X	0
1	0	X	0	1

$D_C=ABC'$



8.5

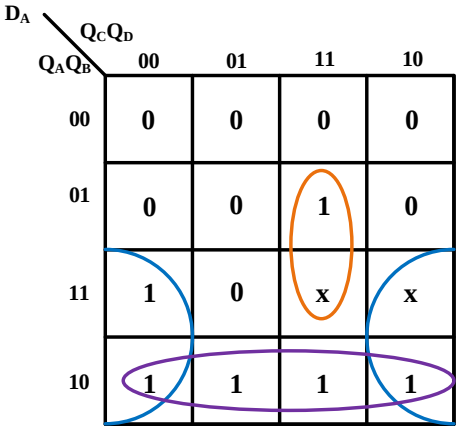
Solution 1 (鎖在 1101):



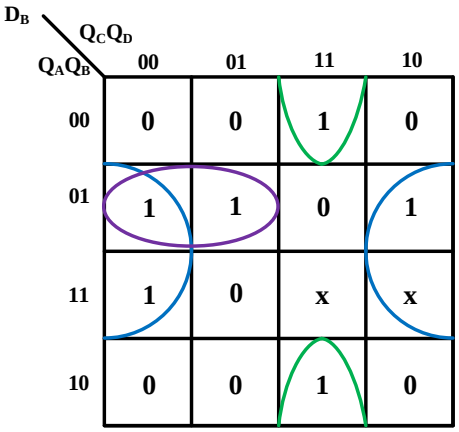
Q3	Q2	Q1	Q0	D3	D2	D1	D0
0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	0
0	0	1	0	0	0	1	1
0	0	1	1	0	1	0	0
0	1	0	0	0	1	0	1
0	1	0	1	0	1	1	0
0	1	1	0	0	1	1	1
0	1	1	1	1	0	0	0
1	0	0	0	1	0	0	1
1	0	0	1	1	0	1	0
1	0	1	0	1	0	1	1
1	0	1	1	1	1	0	1
1	1	0	1	1	1	0	1

Solution 2 (1101 後重新數):

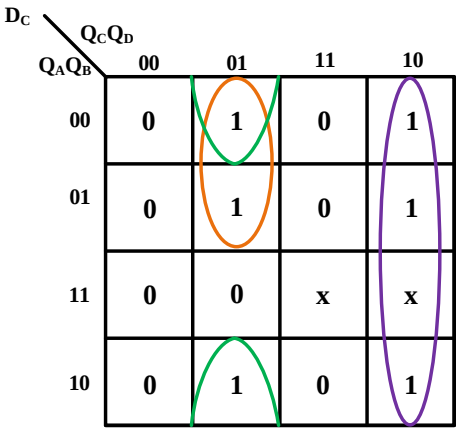
Q_A	Q_B	Q_C	Q_D	D_A	D_B	D_C	D_D
0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	0
0	0	1	0	0	0	1	1
0	0	1	1	0	1	0	0
0	1	0	0	0	1	0	1
0	1	0	1	0	1	1	0
0	1	1	0	0	1	1	1
0	1	1	1	1	0	0	0
1	0	0	0	1	0	0	1
1	0	0	1	1	0	1	0
1	0	1	0	1	0	1	1
1	0	1	1	1	1	0	1
1	1	0	1	0	0	0	0



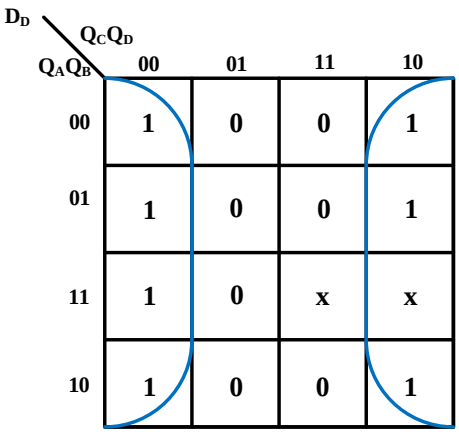
$D_A=Q_AQ_B'+Q_AQ_D'+Q_BQ_CQ_D$



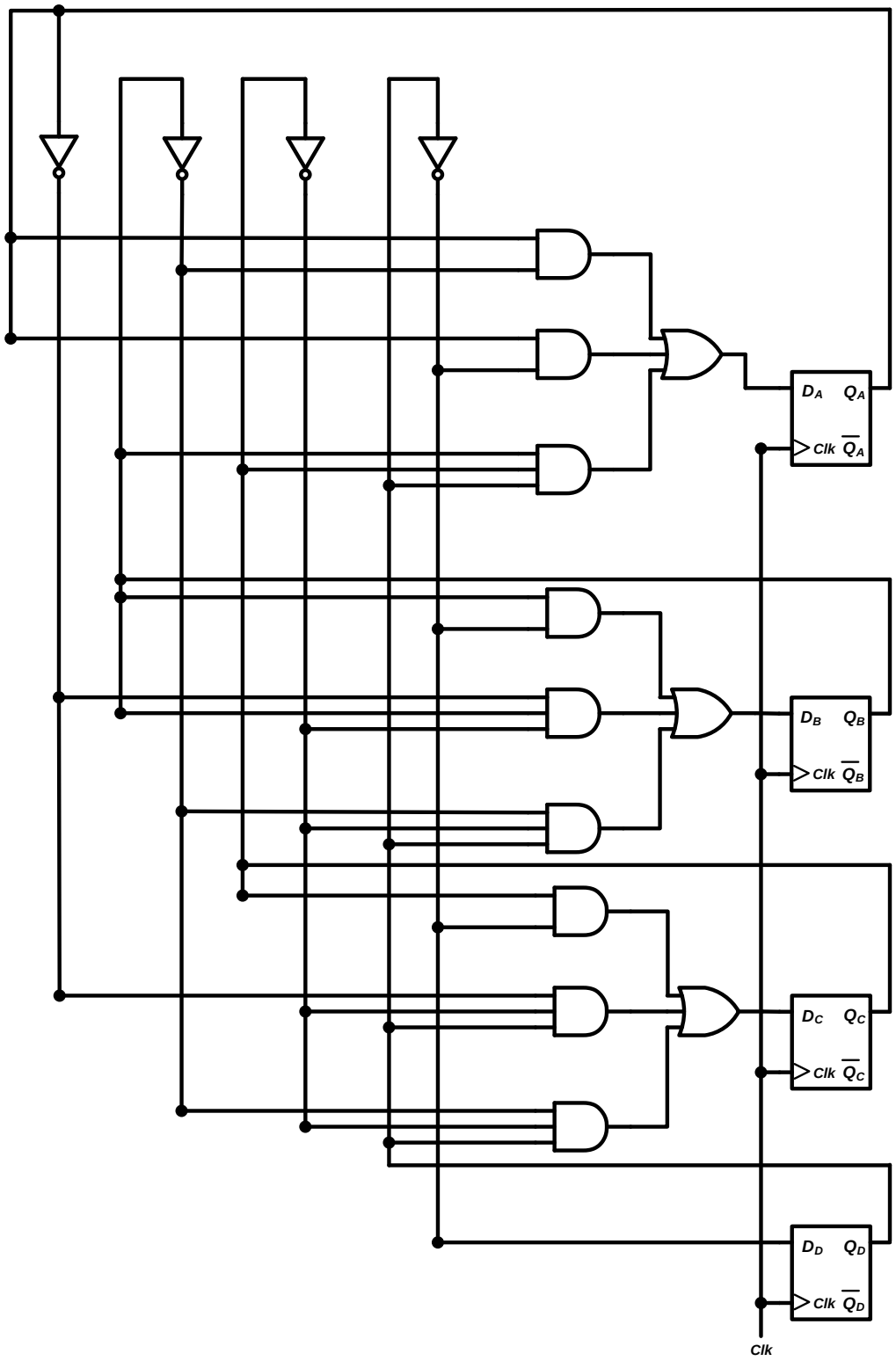
$D_B=Q_BQ_D'+Q_A'Q_BQ_C'+Q_B'Q_CQ_D$



$D_C=Q_CQ_D'+Q_A'Q_C'Q_D+Q_B'Q_C'Q_D$

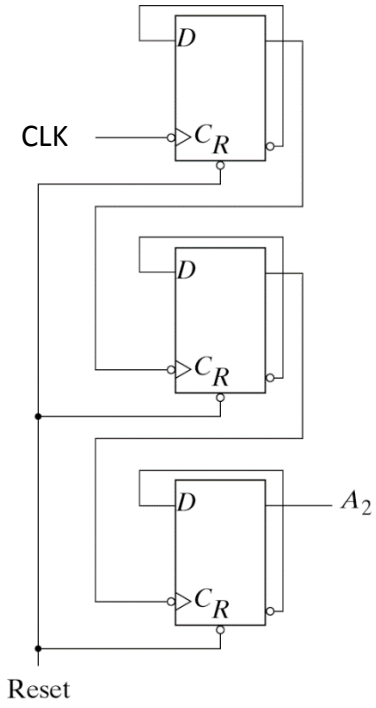


$D_A=Q_D'$


D_A
Q_A
Clk
$\overline{Q}_A$
D_B
Q_B
Clk
$\overline{Q}_B$
D_C
Q_C
Clk
$\overline{Q}_C$
D_D
Q_D
Clk
$\overline{Q}_D$
Clk

8.6

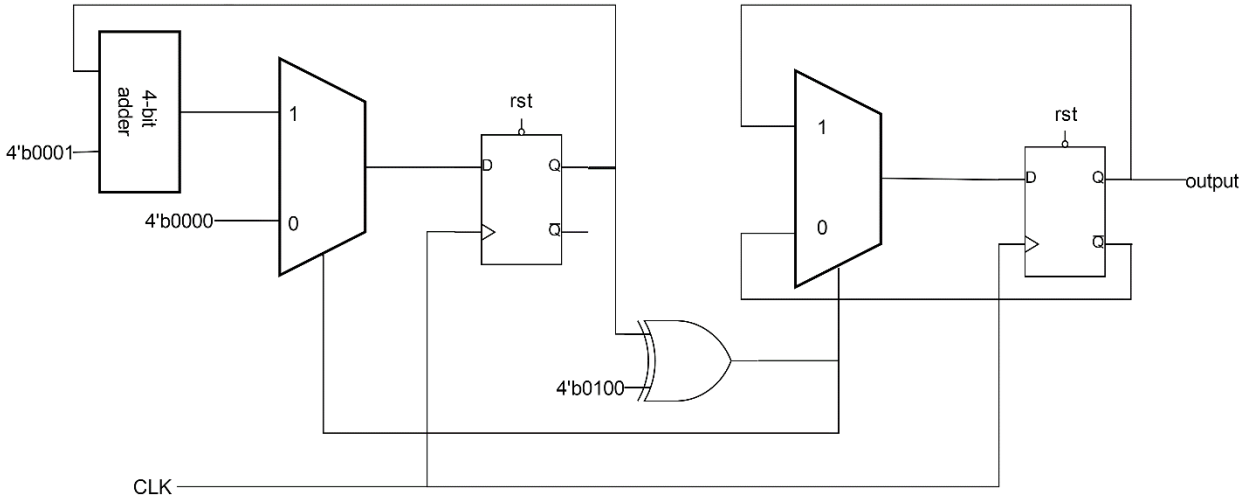
(1)



(2)

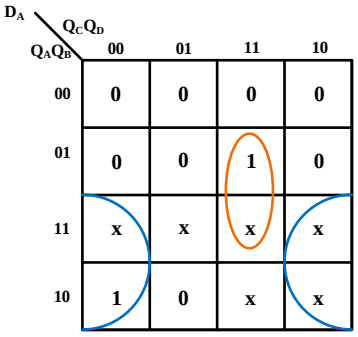
方法 1.

說明: 前半段累加器，每個周期加一，加到 4(0100)後，XOR gate 的輸出會為零。此時第一個 MUX 選擇 0 而不是加法器的輸出。形成 0000、0001、0010、0011、0100、0000、0001…循環。第二個多功器則會每五個週期反向一次，形成 1/10 的除頻器。

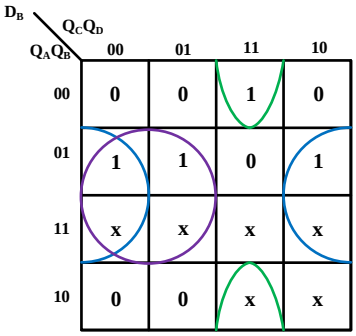


方法 2.

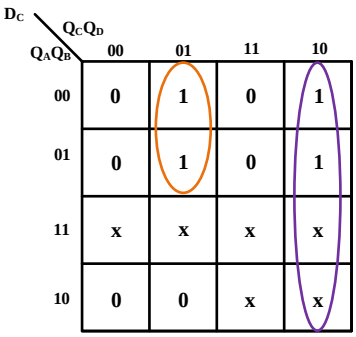
Q_A	Q_B	Q_C	Q_D	D_A	D_B	D_C	D_D	Out
0	0	0	0	0	0	0	1	0
0	0	0	1	0	0	1	0	0
0	0	1	0	0	0	1	1	0
0	0	1	1	0	1	0	0	0
0	1	0	0	0	1	0	1	0
0	1	0	1	0	1	1	0	1
0	1	1	0	0	1	1	1	1
0	1	1	1	1	0	0	0	1
1	0	0	0	1	0	0	1	1
1	0	0	1	0	0	0	0	1



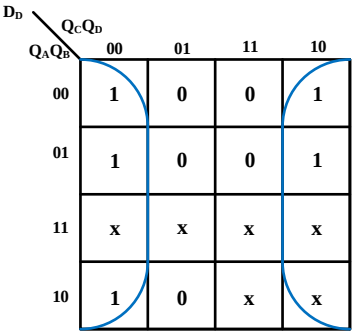
$D_A=Q_AQ_D'+Q_BQ_CQ_D$



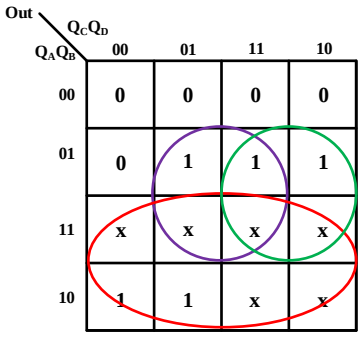
$D_B=Q_BQ_D'+Q_BQ_C'+Q_B'Q_CQ_D$



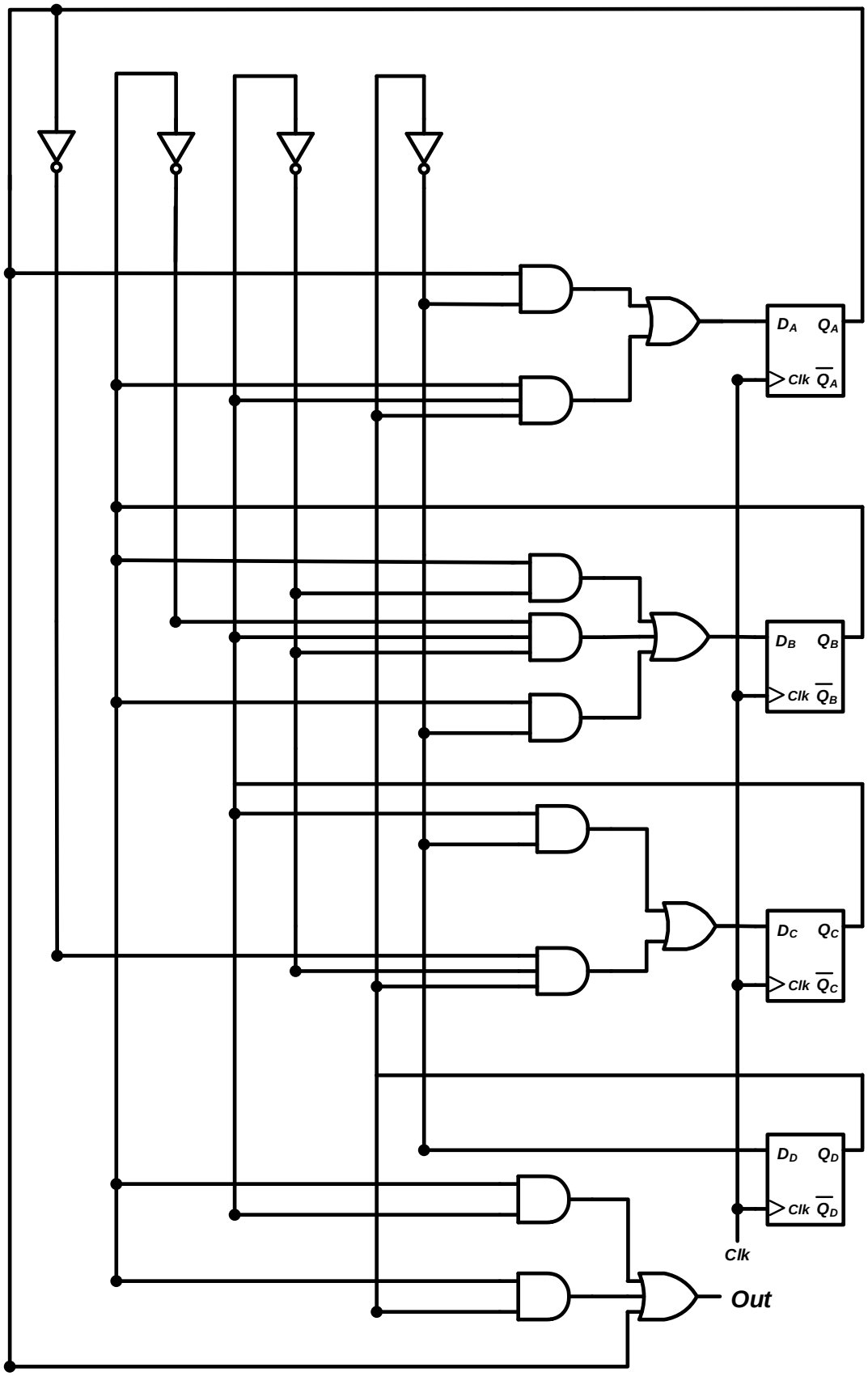
$D_C=Q_CQ_D'+Q_A'Q_C'Q_D$



$D_A=Q_D'$

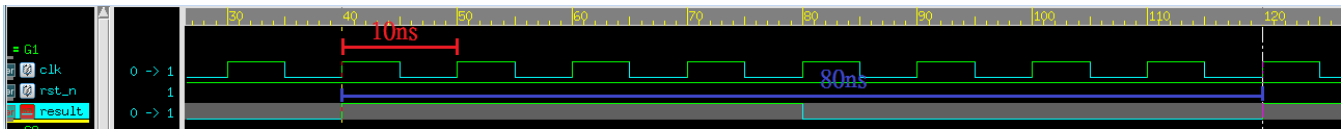


$D_B=Q_A+Q_BQ_C+Q_BQ_D$

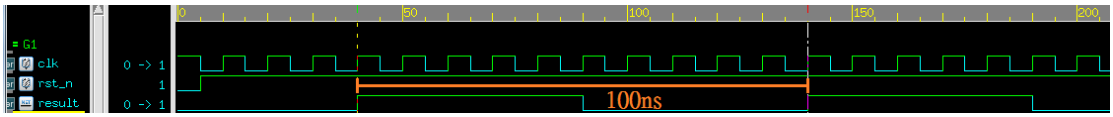

D_A Q_A
Clk $\overline{Q_A}$
D_B Q_B
Clk $\overline{Q_B}$
D_C Q_C
Clk $\overline{Q_C}$
D_D Q_D
Clk $\overline{Q_D}$
Clk
Out

8.7

(a)



(b)



8.8

8,(a)

Shift	State
0	1000
1	0100
2	0010
3	0001
4	1000

8(b)

Shift	State
0	10.....0
1	010.....0
2	0010....0
⋮	⋮
n-1	00.....1

∴ n states