HW8

1. The content of a 5-bit shift register is initially 10101. The register is shifted five times to the left with the serial input 10101 (left bit is first input). What is the content of the register after *each shift*?
2. Draw the logic diagram of a four-bit register with four D flip-flops and four 4x1 multiplexers with mode selection S1 and S0. The register operates according to the following function table.

S1	S0	Register Operation
0	0	Load parallel data
0	1	Complement the four outputs
1	0	Clear register to 0 (synchronous with the clock)
1	1	No change

3. Show that a Johnson counter with n flip-flops produces a sequence of 2n states. List the 10 states produced with five flip-flops and the Boolean terms of each of the 10 AND gate outputs.

4. Use D flip-flops and gates to design a binary counter with each of the following repeated binary sequences:

   (a) 1, 4, 7

   (b) 0, 2, 4, 6, 7

5. Use D flip-flops and gates to design a synchronous binary counter that counts from 0000 to 1101.

6. Frequency divider:

(a) Design a frequency divider to provide the output signal with frequency as 1/8 of the that of the original signal.

(b) Design a frequency divider to provide the output signal with frequency as 1/10 of the that of the original signal.

7. Use Verilog to verify the frequency divider in Prob. 6 with simulation results.

8. A ring counter is a shift register, as in Figure 7-9, with the serial output connected to the serial input.

(a) Starting from an initial state of 1000, list the sequence of states of the four flip-flops after each shift.

(b) Beginning in state 10…0, how many states are there in the count sequence of an *n*-bit ring counter?