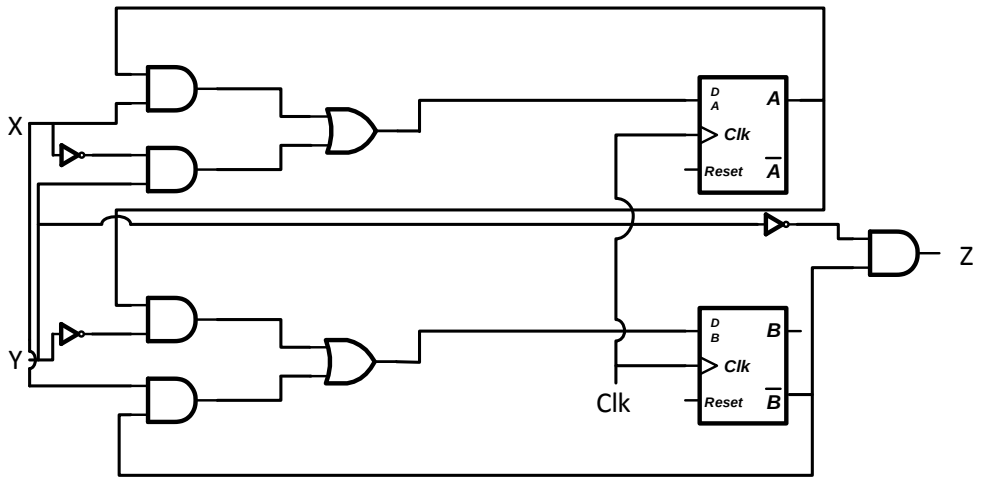
1.

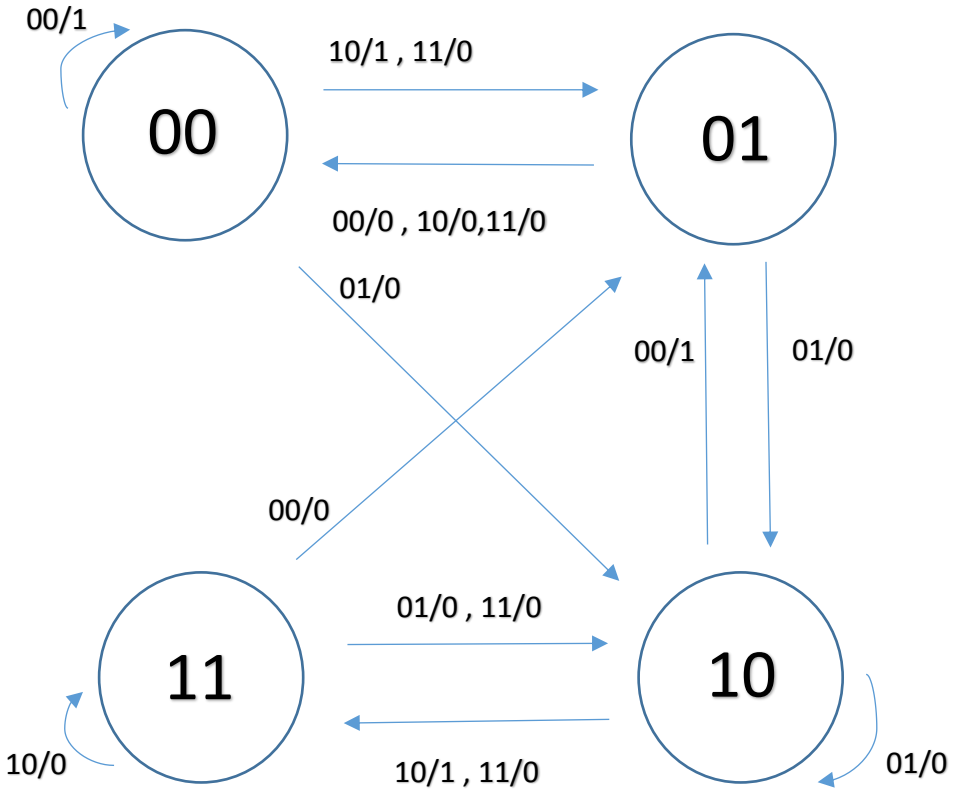
a.)



b.)

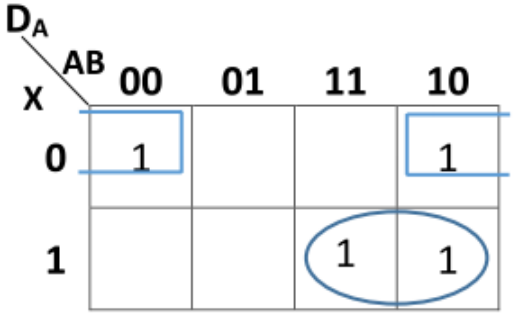
Present state		Input		Next Stage		Output
A	**B**	**X**	**Y**	**A+1**	**B+1**	**Z**
0	0	0	0	0	0	1
0	0	0	1	1	0	0
0	0	1	0	0	1	1
0	0	1	1	0	1	0
0	1	0	0	0	0	0
0	1	0	1	1	0	0
0	1	1	0	0	0	0
0	1	1	1	0	0	0
1	0	0	0	0	1	1
1	0	0	1	1	0	0
1	0	1	0	1	1	1
1	0	1	1	1	1	0
1	1	0	0	0	1	0
1	1	0	1	1	0	0
1	1	1	0	1	1	0
1	1	1	1	1	0	0

c.)

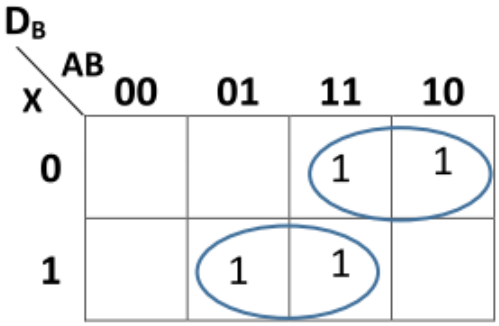


2.

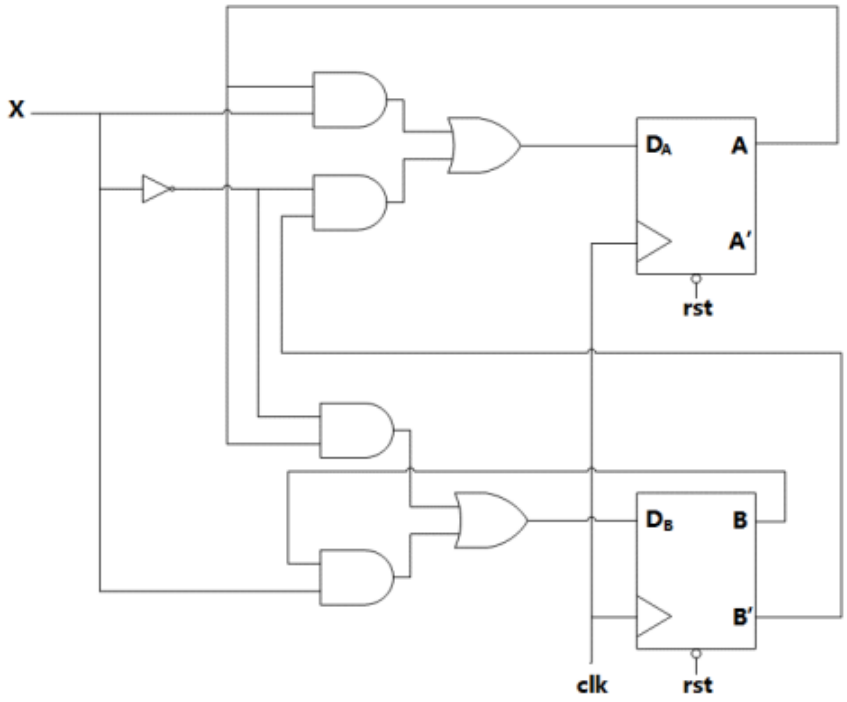
Present state		Input	Next state	
A	B	x	A+1	B+1
0	0	0	1	0
0	0	1	0	0
0	1	0	0	0
0	1	1	0	1
1	0	0	1	1
1	0	1	1	0
1	1	0	0	1
1	1	1	1	1



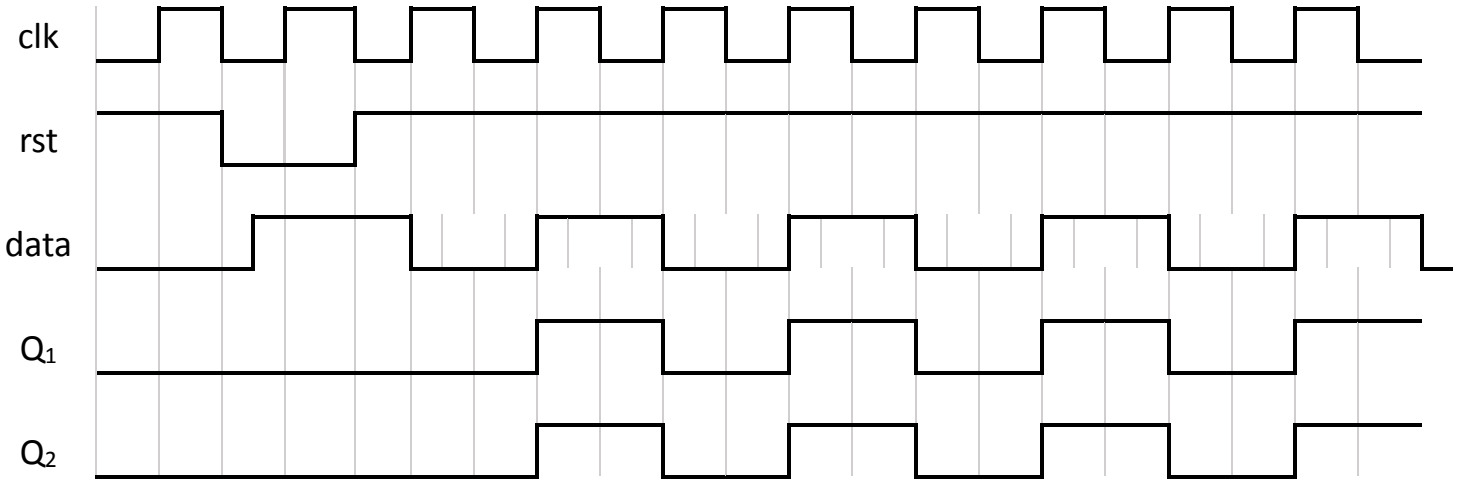
$D_A = B'X' + AX$



$D_B = AX' + BX$



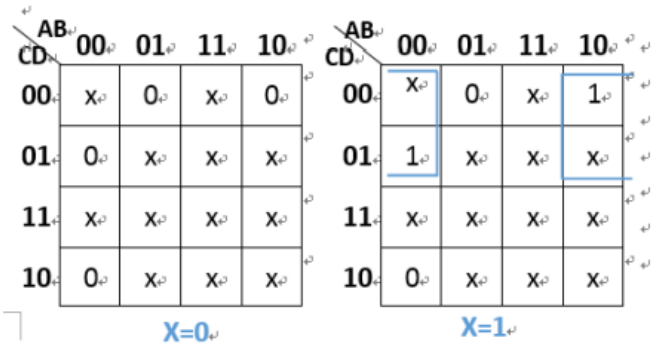
3.



4.

00→1000 01→0100 10→0010 11→0001

Present state				Input	Next state				Output
A	B	C	D	x	A+1	B+1	C+1	D+1	Y
1	0	0	0	0	0	1	0	0	1
1	0	0	0	1	1	0	0	0	1
0	1	0	0	0	0	1	0	0	0
0	1	0	0	1	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0
0	0	1	0	1	0	0	1	0	0
0	0	0	1	0	0	0	0	1	0
0	0	0	1	1	1	0	0	0	0



$D_A = B'C'X$

AB / CD	00	01	11	10
00	x	1	x	1
01	0	x	x	x
11	x	x	x	x
10	0	x	x	x

X=0

AB / CD	00	01	11	10
00	x	0	x	0
01	0	x	x	x
11	x	x	x	x
10	0	x	x	x

X=1

$D_B = C'D'X'$

AB / CD	00	01	11	10
00	x	0	x	0
01	0	x	x	x
11	x	x	x	x
10	0	x	x	x

X=0

AB / CD	00	01	11	10
00	x	1	x	0
01	0	x	x	x
11	x	x	x	x
10	1	x	x	x

X=1

$D_C = A'D'X$

AB / CD	00	01	11	10
00	x	0	x	0
01	1	x	x	x
11	x	x	x	x
10	1	x	x	x

X=0

AB / CD	00	01	11	10
00	x	0	x	0
01	0	x	x	x
11	x	x	x	x
10	0	x	x	x

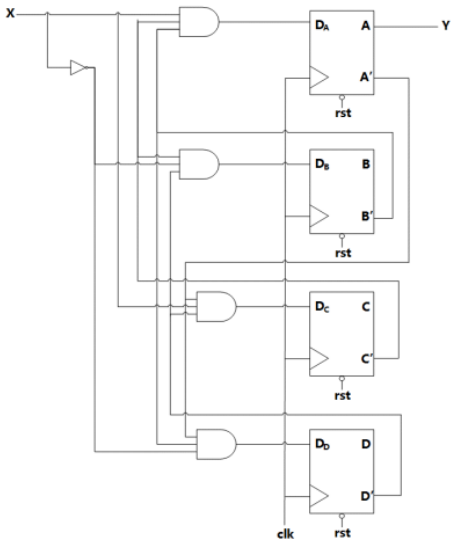
X=1

$D_D = A'B'X'$

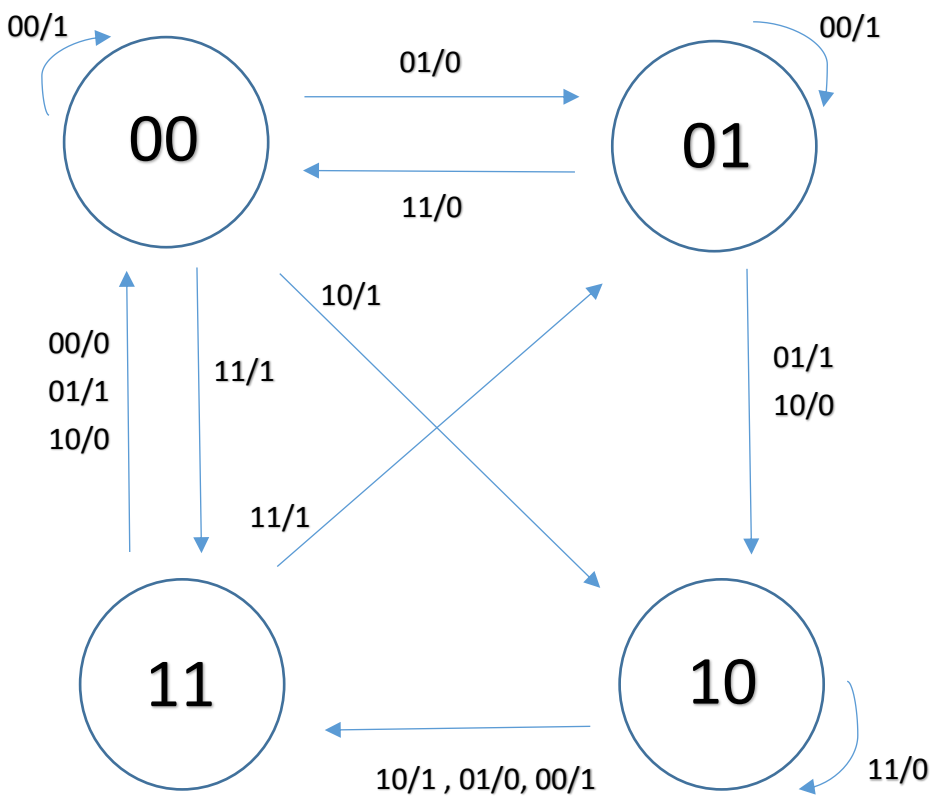
AB / CD	00	01	11	10
00	x	0	x	1
01	0	x	x	x
11	x	x	x	x
10	0	x	x	x

AB / CD	00	01	11	10
00	x	0	x	1
01	0	x	x	x
11	x	x	x	x
10	0	x	x	x

$Y = A$



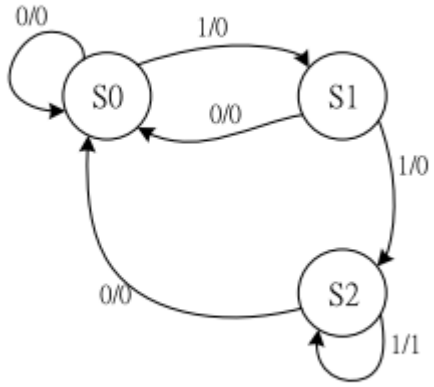
5.


00/1
00
01/0
11/0
01
00/1
10/1
00/0
01/1
10/0
11/1
11/1
01/1
10/0
11
10
10/1 , 01/0, 00/1
11/0

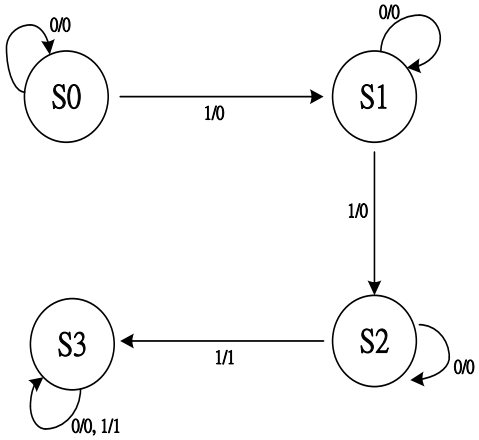
6.

(a)

Case1: 連續的 1



Case2: 不連續的 1



(b)

Case1

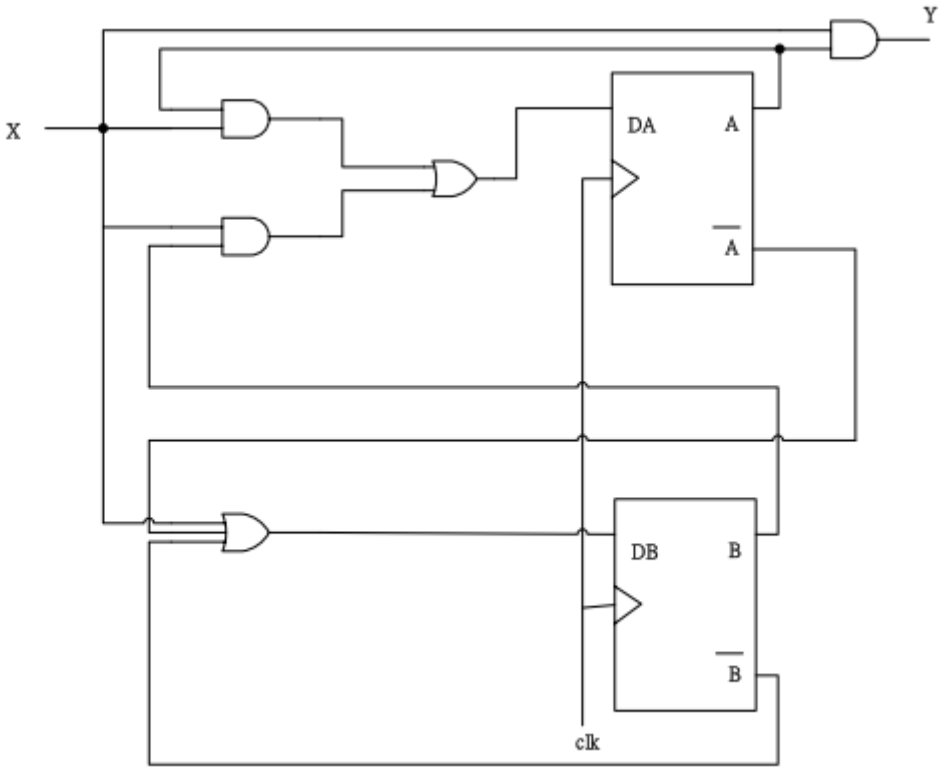
Present state		Input	Next state		output
A	**B**	**x**	**A+1**	**B+1**	**Y**
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	1	0	0
1	0	0	0	0	0
1	0	1	x	x	1

Case2

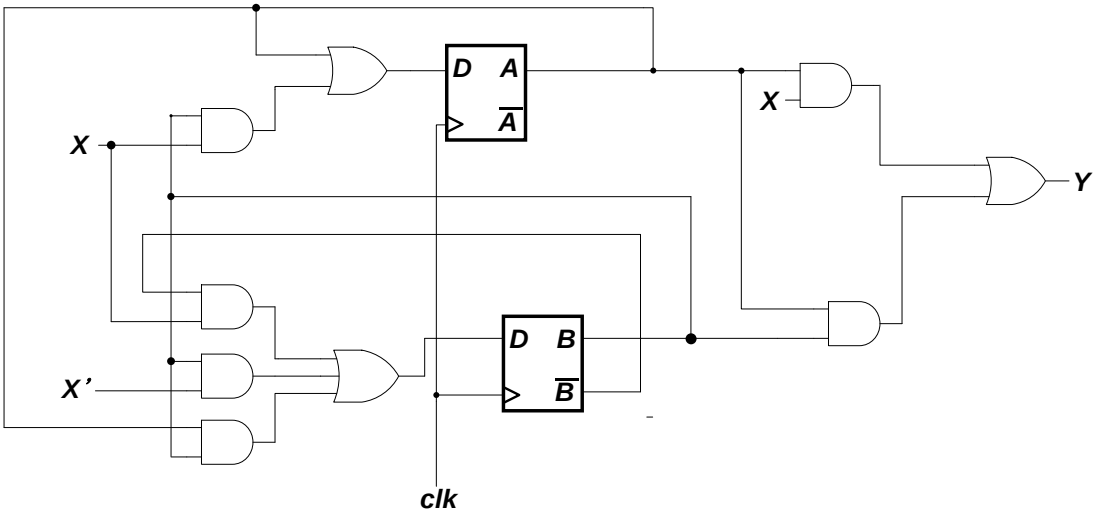
Present state		Input	Next state		output
A	**B**	**x**	**A+1**	**B+1**	**Y**
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	1	0
0	1	1	1	0	0
1	0	0	1	0	0
1	0	1	1	1	1
1	1	0	1	1	1
1	1	1	1	1	1

(c)

Case1



Case2



7.

```
module Hw7_7(DA,DB,A,B,x);
output DA,DB;
input A,B,x;
assign DA = ((~B) & (~x)) | (A & x);
assign DB = (A & (~x)) | (B & x);
endmodule
```

.v檔

```
module test_Hw7_7;
wire DA,DB;
reg A,B,x;

Hw7_7 U0(.DA(DA),.DB(DB),.A(A),.B(B),.x(x));
initial
begin
    A=0;B=0;x=0;
    #10 A=0;B=0;x=1;
    #10 A=0;B=1;x=0;
    #10 A=0;B=1;x=1;
    #10 A=1;B=0;x=0;
    #10 A=1;B=0;x=1;
    #10 A=1;B=1;x=0;
    #10 A=1;B=1;x=1;
end
endmodule
```

testbench檔

8.

Reduced state table

Present state	Next state		Output	
	X=0	X=1	X=0	X=1
a	f	b	0	0
b	d	b	1	0
d	d	a	1	0
f	f	b	1	1
h	d	a	0	0

Original table

state	a	b	d	a	b	d	a	f	b	d	g
Input	1	0	1	1	0	1	0	1	0	0	1
Output	0	1	0	0	1	0	0	1	1	1	0

Reduced table

state	a	b	d	a	b	d	a	f	b	d	d
Input	1	0	1	1	0	1	0	1	0	0	1
Output	0	1	0	0	1	0	0	1	1	1	0