

HW6

1. Find the 1's complement and 2's complement of the following binary numbers: 11100001, 10101011, 01110011, 11100111, and 01010101.
2. Performed the addition. The numbers are 2's complement numbers. (a) 0101 + 1110, (b) 0111010 + 1101011. Indicate whether overflow occurs.
3. Perform the subtraction with the following unsigned binary numbers by taking the 2's complement of the subtrahend. (a) 0101 – 0110, (b) 10110 – 1100, (c) 1011110 – 1111110, (d) 101001 – 101.
4. Repeat Problem 3, assuming the numbers are 2's complement signed numbers. Indicate whether overflow occurs.
5. Repeat Problem 3, assuming the numbers are signed-magnitude signed numbers. Indicate whether overflow occurs.
6. Design a 4-bit signed-magnitude adder-subtractor. Divide the circuit for the design into (1) sign generation and add-subtract control logic, (2) an unsigned number adder-subtractor using 2's complement of the minuend for subtraction, and (3) selective 2's complement result correction logic.
7. Design a 4-bit absolute value calculator, $Z=|z|$.
8. Design a multiplier that multiplies two 3-bit 2's complement signed numbers.
9. Design a combinational circuit that compares two 4-bit unsigned numbers A and B to see whether A is greater than B. The circuit has one output X such that $X = 0$ if $A \leq B$ and $X = 1$ if $A > B$.
10. Use Verilog to design the circuit in problem 9.