HW5

1. Implement a 5 -> 32 decoder using a 2->4 decoder and a 3->8 decoder.

2. Design a three-way magnitude comparator that outputs true if its three inputs are in strict order: a>b>c.

3. Design an arbiter with programmable priority – a binary input selects which bit is highest priority. The priority rotates rightward from that bit position. The input/output bit number of the arbiter is 4.

4. Use Verilog to simulate the arbiter in problem 3.

5. Design an 8->1 multiplexer using a 3->8 decoder and 8x2 AND-OR.

6. Use Verilog to simulate the multiplexer in problem 5.

7. Draw the logic diagram of a 3->8 decoder using only NOR and NOT gates.

8. Design a 4->2 priority encoder with input D[3:0] and output A[1:0] where D_0 has the highest priority and D_3 has the lowest priority.

