HW4

1. Optimize the following Boolean function F together with the don't-care conditions d.

$$F(w,x,y,z) = \Pi(0,1,3,4,5,6,9,15) + d(5,9,15)$$

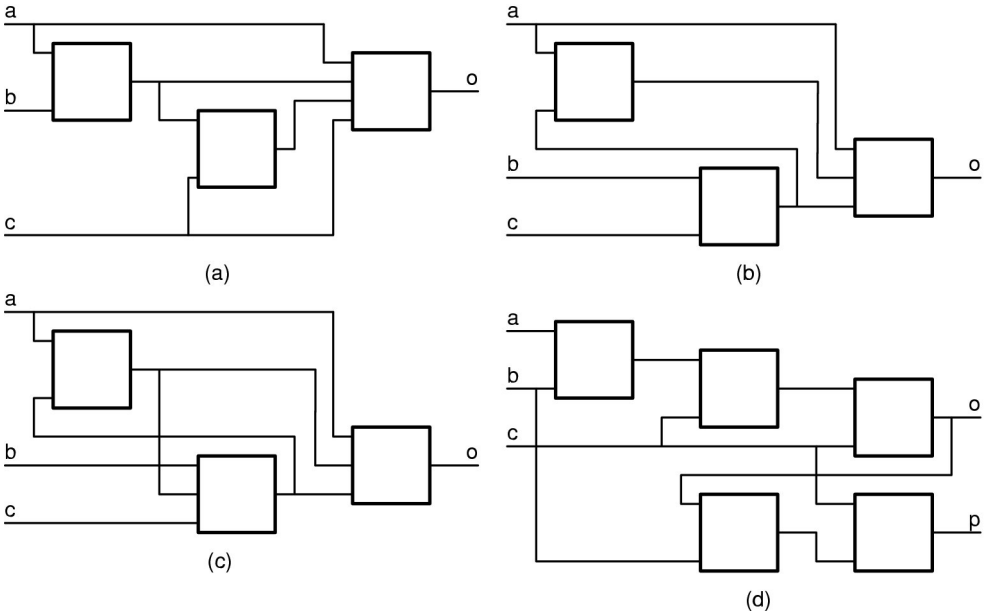
(a) Optimize the function in the form of sum-of-products.

(b) Optimize the function in the form of product-of-sums.

(c) Implement the function using only NAND and NOT gates. Draw the logic diagram.

(d) Find the prime implicants and essential prime implicants of the function.

2. Which of the circuits are combinational? Each of the boxes is itself a combinational circuit.



3. Majority Indicator: Design a voting machine for three people. When there is more than one person agree on some case (with input 1), the case will be passed (with output 1); otherwise, the case will be rejected (with output 0).

(a) Derive the truth table.

(b) Derive the simplified Boolean expressions for A, B, and C using maps.

(c) Draw the related logic diagram.

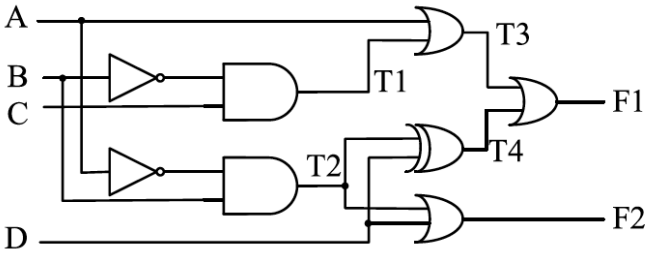
(d) Find the prime implicants and essential prime implicants of the function.

4. Consider the combination circuit shown in the following figure.

(a) Derive the Boolean expressions for T1 through T4. Evaluate the outputs F1 and F2 as a function of four inputs.

(b) List the truth table with 16 binary combinations of the four input variables. Then, list the binary values for T1 through T4 and outputs F1 and F2 in the table.

(c) Plot the output Boolean functions obtained in part (b) on maps and show that the simplified Boolean expressions are equivalent to the ones obtained in part (a).



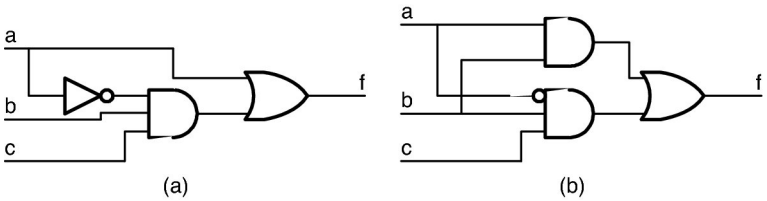
5. Simplify the following expression and implement it with two-level NOR gates.

$$F(w,x,y,z) = \mathrm{w'xyz'} + \mathrm{wx'y'z} + \mathrm{wxy'z'} + \mathrm{w'xy'z}$$

6. Simplify the following expression and implement it with two-level NAND gates.

$$F(x,y,z) = (\mathrm{x'} + \mathrm{y'} + \mathrm{z'})(\mathrm{y'} + \mathrm{z'})(\mathrm{x'} + \mathrm{z'})$$

7. Fix the hazard that may occur in the following figures.



8. A half adder is a circuit that takes in one-bit binary numbers a and b, and outputs a sum s and a carry out co. The concatenation of xo and s, is the two-bit value that results from adding a and b (e.g. if a=1, b=1, s=0, and co=1).

   (a) Derive the truth table of a half adder.

   (b) Derive the Boolean expression of co and s in the simplest sum-of-product form.

   (c) Find the prime implicants and essential prime implicants of co and s.

9. Use Verilog to simulate the half adder in problem 8.

10. Use Verilog to simulate the majority detector in problem 3.

