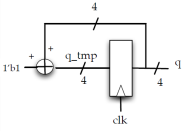
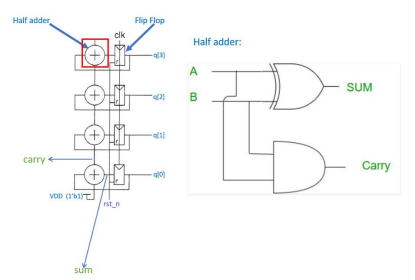
1.

1.1

Block diagram:



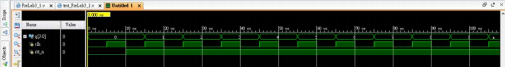
Logic diagram:

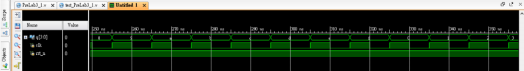
1.2

Input: clk, rst\_n

Output: [3:0]q;

waveform:



As the simulation waveform shows, q is increasing from 0, 1, 2, 3…15, then back to 0,

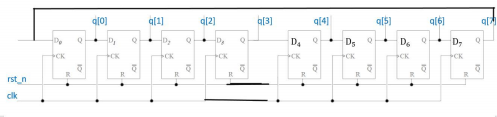
1… etc.

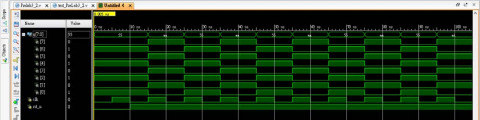
2.

Input: clk, rst\_n

Output: [7:0]q;

Logic diagram:



As the initial value is 8’b0101\_0101, and it’s also ring counter, there is only two

possible value for output ([7:0]q), which is 8’b0101\_0101 and 8’b1010\_1010.