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VGA Port

VGA





VGA

- VGA = Video Graphics Array
- Introduced by IBM in 1987, and still used today
- Transmitting analog signal







Cathode-Ray Tube Monitor

Video Graphics Array DE-15 female and male connector

LED Monitor



VGA Video Signal

• A VGA video signal contains 5 active signals (RGBHV)

- horizontal sync (HS): used for video synchronization in the horizontal direction
- vertical sync (VS): used for video synchronization in the vertical direction
- red (R): used to control the red color, 0v (fully off) $\sim 0.7v$ (fully on)
- green (G): used to control the green color, 0v (fully off) ~ 0.7v (fully on)

Basys 3 bibles (Bard Reference Manuarol the blue color, 0v (fully off) ~ 0.72 bidly en on)



Pin 1: Red	Pin 5: GND
Pin 2: Grn	Pin 6: Red GND
Pin 3: Blue	Pin 7: Grn GND
Pin 13: HS	Pin 8: Blu GND
Pin 14: VS	Pin 10: Sync GNE



Basys 3 Control Signals for VGA

• 14 FPGA pins

-4-bits per color (R, G, B)

-2 standard sync signals (HS, VS)

##VGA Connector

set property PACKAGE PIN G19 [get ports {vgaRed[0]}] set property IOSTANDARD LVCMOS33 [get ports {vgaRed[0]}] set property PACKAGE PIN H19 [get ports {vgaRed[1]}] set property IOSTANDARD LVCMOS33 [get ports {vgaRed[1]}] set property PACKAGE PIN J19 [get ports {vgaRed[2]}] set property IOSTANDARD LVCMOS33 [get ports {vgaRed[2]}] set property PACKAGE PIN N19 [get ports {vgaRed[3]}] set property IOSTANDARD LVCMOS33 [get ports {vgaRed[3]}] set property PACKAGE PIN N18 [get ports {vgaBlue[0]}] set property IOSTANDARD LVCMOS33 [get ports {vqaBlue[0]}] set_property PACKAGE_PIN_L18 [get_ports {vgaBlue[1]}] set property IOSTANDARD LVCMOS33 [get ports {vgaBlue[1]}] set property PACKAGE PIN K18 [get ports {vgaBlue[2]}] set property IOSTANDARD LVCMOS33 [get ports {vgaBlue[2]}] set property PACKAGE PIN J18 [get ports {vgaBlue[3]}] set property IOSTANDARD LVCMOS33 [get ports {vgaBlue[3]}] set property PACKAGE PIN J17 [get ports {vgaGreen[0]}] set property IOSTANDARD LVCMOS33 [get ports {vgaGreen[0]}] set property PACKAGE PIN H17 [get ports {vgaGreen[1]}] set property IOSTANDARD LVCMOS33 [get ports {vqaGreen[1]}] set_property PACKAGE_PIN G17 [get_ports {vgaGreen[2]}] set property IOSTANDARD LVCMOS33 [get ports {vgaGreen[2]}] set property PACKAGE PIN D17 [get ports {vgaGreen[3]}] set property IOSTANDARD LVCMOS33 [get ports {vgaGreen[3]}] set property PACKAGE PIN P19 [get ports hsync] set property IOSTANDARD LVCMOS33 [get ports hsync] set property PACKAGE PIN R19 [get ports vsync] set property IOSTANDARD LVCMOS33 [get ports vsync]







• Cathode Ray Tube (CRT) is a vacuum tube containing one or more electron guns, and a phosphorescent screen is used to view images.



GA Board Reference Manual







VGA System Timing (1/3)

- Whether the information is displayed
 - Displayed: beam moving forward (left to right and top to bottom)
 - Not displayed: the time the beam is reset back to the left or top edge of the display. (Blanking period) HD: 1920*1080 pixels
- Display resolution is determined by 4K: 3840*2160 pixels
 - the size of the beams

assume a object has fixed pixel, it would get smaller as the resolution increases

- the frequency at which the beam can be traced across the display
- the frequency at which the electron beam can be modulated





VGA System Timing (3/3)

Signal timing for a 640-pixel by 480 rows display using a 25MHz pixel clock

1/25MHz = 0.04us





480*32 us = 15.3ms (whole line: 32us)

Parameter	Ver. Sync		Hor. Sync		
	Lines	Time(ms)	Pixels	Time(µs)	
Visible area	480	15.3	640	25 0.04*64	40=25
Front porch	10	0.3	16	0.64	
Sync pulse	2	0.064	96	3.8	
Back porch	33	1.05	48	1.9	
Whole line	525	16.7	800	32	

800 pixels裡只顯示640 pixels



Pixel Clock

- The pixel clock defines the time available to display one pixel of information.
- Example: Suppose we want to display an image with 480 rows and 640 columns, and its refresh rate is 60Hz. The pixel clock which will be delivered to VGA screen must be

800*525*60(frame/sec) = 25M (pixel/sec)

800*525 pixels/frame



RGB Bitmap

- A digital color image is composed by a lot of pixels.
- Each pixel contains three R, G, B values to represent the intensity of these three primary colors.



RGB Color Mode

- Three primary colors
 - -Red

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- -Green
- -Blue
- No one of them can be created as the other two.
- Any other color is a combination





RGB Color Cube

- R, G, and B correspond to three axes in 3D space.
- Normalize the relative amounts of R, G and B so that each value varies between 0 and 1.







RGB Bitmap Example (1/2)

Size: 1215*717

Size: 51*51





RGB Bitmap Example (2/2)





(R,G,B) : range from 0 to 255

(31,46,51)	(70,93,101)	(135,163,174)
(76,99,105)	(138,170,181)	(117,153,165)
(141,168,179)	(118,150,161)	(117,151,161)



Demo 1: Block Diagram



valid: 要不要顯示



Demo 2: Block Diagram



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Memory IP (1/5)



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	📑 AXI Vid	eo Direct Memory Access	AXI4, AXI4-Stream	Production	Included	xilinx.com:ip



Memory IP (2/5)

IP: 矽智產

Customize IP lock Memory Generator (8.2)		
IP Symbol Power Estimation Show disabled ports	Component Name blk_mem_gen_1 Basic Port A Options Other Options Summary Interface Type Native Memory Type Single Port RAM Common Clock	Memory Type Single Port RAM
BRAM_PORTA addra[16:0] clka dina[11:0] douta[11:0] wea[0:0]	ECC Type No ECC Enror Injection Pine Single Bit Enror Injection Write Enable Byte Write Enable Byte Size (bitk) Outprist Defines the algorithm used to concatenate the block RAM primitives. Refer datasheet for more information. Algorithm Minimum Area Primitive	 BRAM_PORTA addra[16:0] clka dina[11:0] douta[11:0] wea[0:0]

clka, **addra**...的a指的是RAM第一 個port

we: write enable



Memory IP (3/5)

Generation IP	and Different	
Block Memory Generator (8.2)		Component Name blk_mem_gen_0
🍘 Documentation 🛅 IP Location 🧔 Switch to Defaults		Basic Port A Ontions Other Options Summary
IP Symbol Power Estimation	Component Name blk. mem gen 1	
Show disabled ports	Basic Port A Options Other Options Summary	Nemory Size
	Memory Size	
	Write Width 12 💿 Range: 1 to 4608 (bits)	Write Width 12 🛛 🔀 Ratige: 1 to 4608 (bits)
	Write Depth 76800 Range: 2 to 1048576	Read Width 12 👻
	Read Depth 76800	W. it D. A. 75900 D. D. m. 0 to 1040576
		Write Depth 70000 Con Raige: 2 to 1048576
	Operating Mode Write First Enable Port Type Use ENA Pin	Read Depth 76800
	Poir A Opublici Output Registers Use ENA Pin	
BRAM_PORTA		Operating Mode Write First 👻 Enable Port Type Always Enabled 👻
- >addra[16:0]	Port & Output Reset Options	
- Delka	RSTA Pin (settreset pin) Output Reset Value (Hex) 0	
→dina[11:0]	Reset Memory Latch Reset Priority CE (Latch or Register Enable)	
- douts[11:0]	DEAD Address Charge A	
	READ Address Change A	RGR · 12 hits
wea[0.0]	rear Frances Charles F	KUD . 12 0105
		$320x240 \cdot 76800$
		5201210.10000
		76800*12 bits in total
		UK

1800kbits of fast block RAM in FPGA



Memory IP (4/5)

🖵 Customize IP	and the second se	x
Block Memory Generator (8.2)		
🍘 Documentation 📄 IP Location 🧔 Switch to Defaults		
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Power Estimation Show disabled ports BRAM_PORTA addra[16:0] clka dina[11:0] douta[11:0] wea[0:0]	Commonent Mane Likk men en l Besic Fort A Options Other Options Summary Fipeline Stages within Mux I whux Size: 19x1 Memory Initialization I coal Init File Coe File no.coe file loaded Fill Remaining Memory Locations Remaining Memory Locations Remaining Memory Locations Remaining Memory Locations (Hex) 0 Structural/UniSim Simulation Model Options Defines the type of warnings and outputs are generated when a read-write or write-write collision occurs. Collision Warnings All w Behavioral Simulation Model Options Disable Collision Warnings Disable Out of Range Warnings	Component Name blk_mem_gen_0 Basic Port A Options Other Options Summary Pipeline Stages within Mux I Mux Size: 19x1 Memory Initialization Load Init File Coe File no_coe_file_loaded Coe File no_coe_file_loaded Coe File no_coe_file_loaded Coe File no_coe_file_loaded
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Memory IP (5/5)



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Picture Format Translation (1/2)

out.coe

amumu.jpg	radix:下面115,743都是16進位 1 memory_initialization_radix=16; 2 memory_initialization_vector=
	PicTrans.exe ³ 115, 4 115, 5 115, 6 115, 8 115, 9 115, 10 115, 11 115, 12 115, 2 202 242
	76797 743, 76798 743, 76799 743, 76799 743, 76800 743, 76801 743, 76802 743; 76803 每個位置用逗號隔 76803 開,結束用分號



Picture Format Translation (2/2)

• PicTrans.exe:

-Convert a *.jpg file to a bit map file

• Input:

- -image (*.jpg)
- the width of the output file
- the height of the output file

• Output:

-out.coe





Lab 11: VGA Display



Action Item (1/2)

Modify the Verilog code introduced in class to design a circuit for controlling the VGA display.

• input ports:

input clk; input reset; input en;

• output ports:

output [3:0]vgaRed; output [3:0]vgaGreen; output [3:0]vgaBlue; output hsync; output vsync;



Action Item (2/2)

- At the beginning or when pressing the **reset** button, the VGA display will show the image (e.g., amumu.jpg) at the origin position. It will stay still until the **en** button is pressed.
- The image will start/resume scrolling down row by row under the frequency of clk divided by 2²² (i.e., clk/2²²), or pause, depending on whether the number of the **en** button pressed is odd or even.



Example (1/6)

at the beginning or pressing reset

(0 row scrolled down)





Example (2/6)

press en \rightarrow start to scroll down

(100 rows scrolled down)





Example (3/6)

(200 rows scrolled down)





Example (4/6)

(300 rows scrolled down)





Example (5/6)

(400 rows scrolled down)





Example (6/6)

press en pause

(400 rows scrolled down)

