Pre-Lab5 Report

Ⅰ. Pre-Lab5_1 (FSM simulation)

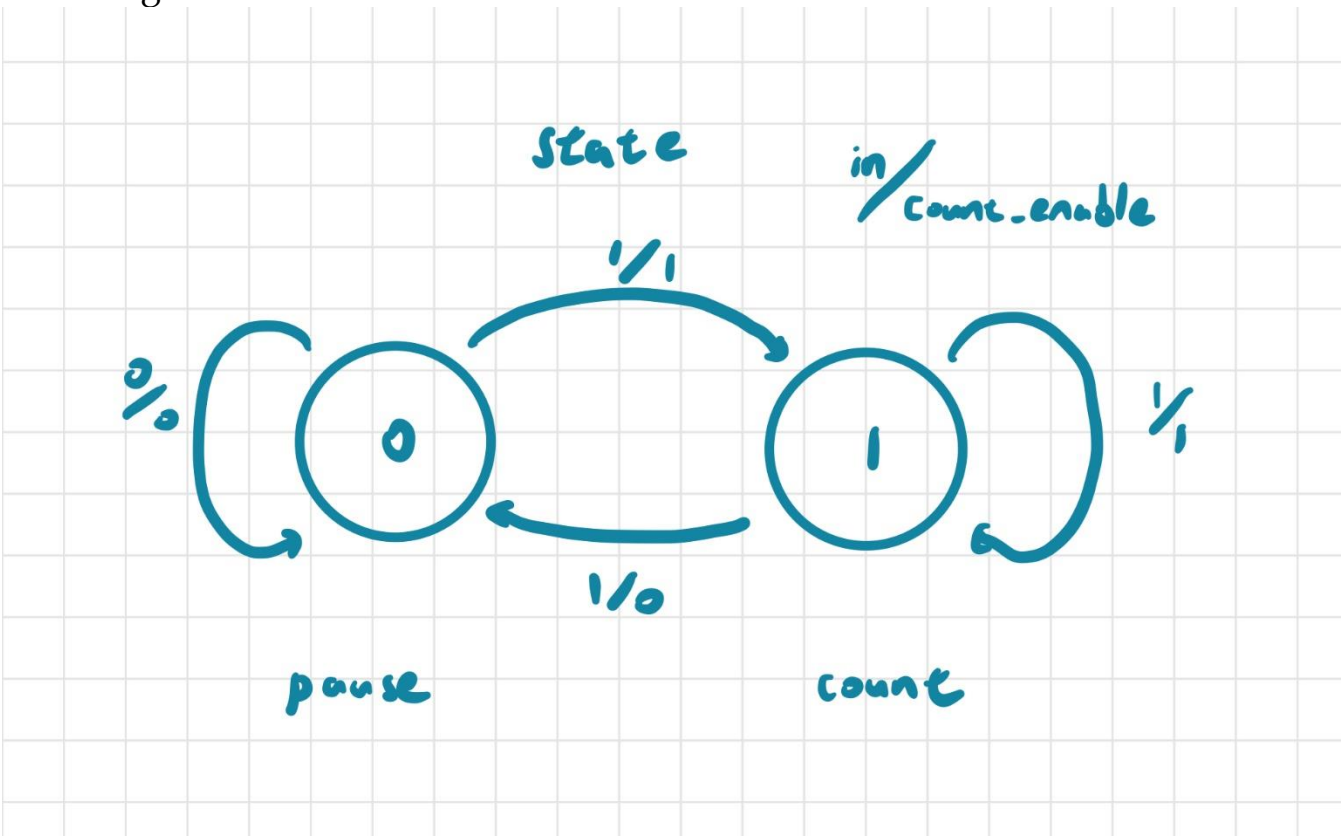
Design Specification

IO:
Input: clk, rst_n, stop (the signal of bottom).
Output: state

Design Implementation

想法是先畫出 state diagram，因為只有 pause 跟 count 兩種 state，所以只需要一個 bit 去表現 state，0 為 pause，1 為 count，我的設計是當按下 reset 不管在什麼狀態都會回到 pause 的狀態，因為題目要求用一顆 LED 來顯示 state，所以在接線時，直接把 state 接到一顆 LED 即可完成題目要求。

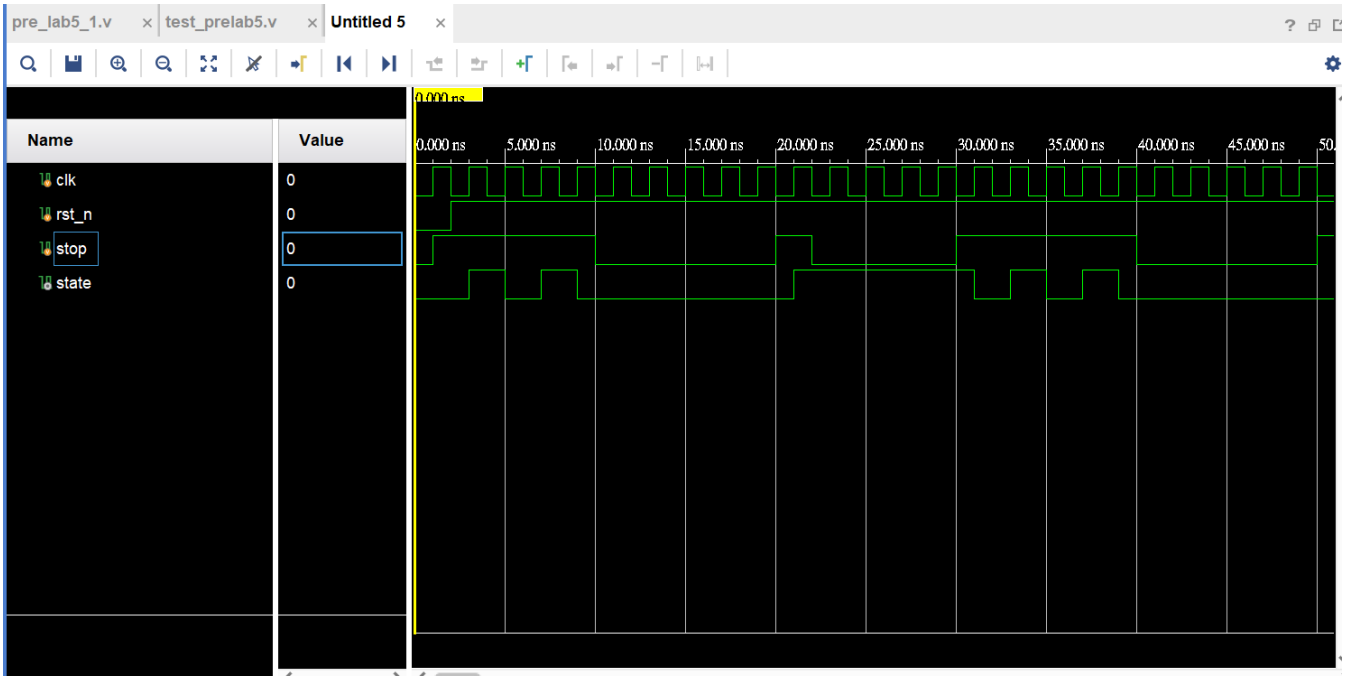
state diagram:



If state = 0 (pause) and signal is 0, then keep the state.
If state = 0 (pause) and signal is 1, then jump to next state (state = 1) (start).
If state = 1 (start) and signal is 0, then keep the state.

If state = 1 (start) and signal is 1, then jump to next state (state = 0) (pause).

Simulation:



我的 stop 就是上述 in 的 signal