Lab 7: Speaker

Objective

- ✓ Learn the timing control via the speaker example.

Prerequisite

- ✓ Fundamentals of logic gates.
- ✓ Counter, Frequency divider.
- ✓ Logic modeling in Verilog HDL.

Experiments

1 Please design an audio-data parallel-to-serial module to generate the speaker control signal with 100MHz system clock, 25 MHz master clock, (25/128) MHz Left-Right clock (Fs), and 6.25 MHz (32Fs) sampling clock.
   1.1 Design a general frequency divider to generate the required frequencies for speaker clock.
   1.2 Design a stereo signal parallel-to-serial processor to generate the speaker control signals. Please use Verilog simulation waveform to verify your control signal.

2 Speaker control
   2.1 Please produce the buzzer sounds of **Do**, **Re**, and **Mi** by pressing buttons (Left, Center, Right) respectively. When you press down the button, the speaker produces corresponding frequency sound. When you release the switch, the speaker stops the sound.
   2.2 Please control the volume of the sound by pressing button (Up) as increase and (Down) and decrease the volume. Please also quantize the audio dynamic range as 16 levels and show the current sound level in the 7-segment display.

