Lab 1: Verilog HDL

Objective

- ✓ Review fundamental logic components.
- ✓ Introduce Verilog HDL modeling and verification.

Prerequisite

- ✓ Fundamentals of logic gates and Verilog HDL.

Experiments

1 Design and verify a BCD-to-Excess-3 code converter (input: ***abcd***, output: ***wxyz***, ***a*** and ***w*** are the MSB).
- 1.1 Write the Boolean function/logic equation.
- 1.2 Draw the related logic diagram.
- 1.3 Construct the Verilog RTL code for the converter and use a testbench to simulate the logic behavior for verification.

2 Design and verify an unsigned 2-bit x 2-bit binary multiplier (multiplicand ***a*** ($\mathbf{a}_1\mathbf{a}_0$), multiplier ***b*** ($\mathbf{b}_1\mathbf{b}_0$), and product ***c*** ($c_3c_2c_1c_0$)).
- 2.1 Write the Boolean function/logic equation.
- 2.2 Draw the related logic diagram.
- 2.3 Construct the Verilog RTL code for the multiplier and use a testbench to simulate the logic behavior for verification.

3 Design a 3-bit binary adder/subtractor with input ***a*** ($\mathbf{a}_2\mathbf{a}_1\mathbf{a}_0$), ***b*** ($\mathbf{b}_2\mathbf{b}_1\mathbf{b}_0$), **m** as the operator control (0 for addition and 1 for subtraction); output ***s*** ($\mathbf{s}_2\mathbf{s}_1\mathbf{s}_0$), **v** as overflow indicator.
- 3.1 Write the Boolean function/logic equation.
- 3.2 Draw the related logic diagram.
- 3.3 Construct the Verilog RTL code for the function and use a given testbench to simulate the logic behavior for verification.

4 (Bonus) For two 3-bit unsigned numbers ***a*** ($\mathbf{a}_2\mathbf{a}_1\mathbf{a}_0$) and ***b*** ($\mathbf{b}_2\mathbf{b}_1\mathbf{b}_0$), build a logic circuit to output ***o***($o_2o_1o_0$) as the smaller number and use a given testbench for verification.

