Lab 2: FPGA Emulation

Objective

- ✓ Introduce BASYS3 demo board emulation flow.

Prerequisite

- ✓ Fundamentals of logic gates.
- ✓ Verilog HDL representation of Logic components.

Experiments

1 Emulate exp1 in lab1 (a full adder ***s***+***cout***=***x***+***y***+***cin***) with the following parameters.

I/O	***x***	***y***	***cin***	***s***	***cout***
LOC	V17	V16	W16	U16	E19

2 Derive a BCD (***i***[3:0]) to 7-segment display decoder (***D_ssd***[7:0]), and also use four LEDs (***d***[3:0]) to monitor the 4-bit BCD number. (Other values of ***i*** outside the range will show F).

3 Derive a binary (***i***[3:0], 0-9, a, b, c, d, e, f) to 7-segment display decoder (***D***[7:0]), and also use four LEDs (***d***[3:0]) to monitor the 4-bit binary number.

4 (Bonus) Design a combinational circuit that compares two 4-bit unsigned numbers A and B to see whether A is greater than B. The circuit has one output X such that X = 0 if A ≤ B and X = 1 if A > B. (let A[3:0], B[3:0] be controlled by 8 DIP switches, the binary numbers are displayed on 8 LEDs. The result X is on another LED.)

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