



# EECS 207002

## Logic Design Laboratory

### 邏輯設計實驗

## Vivado Simulation

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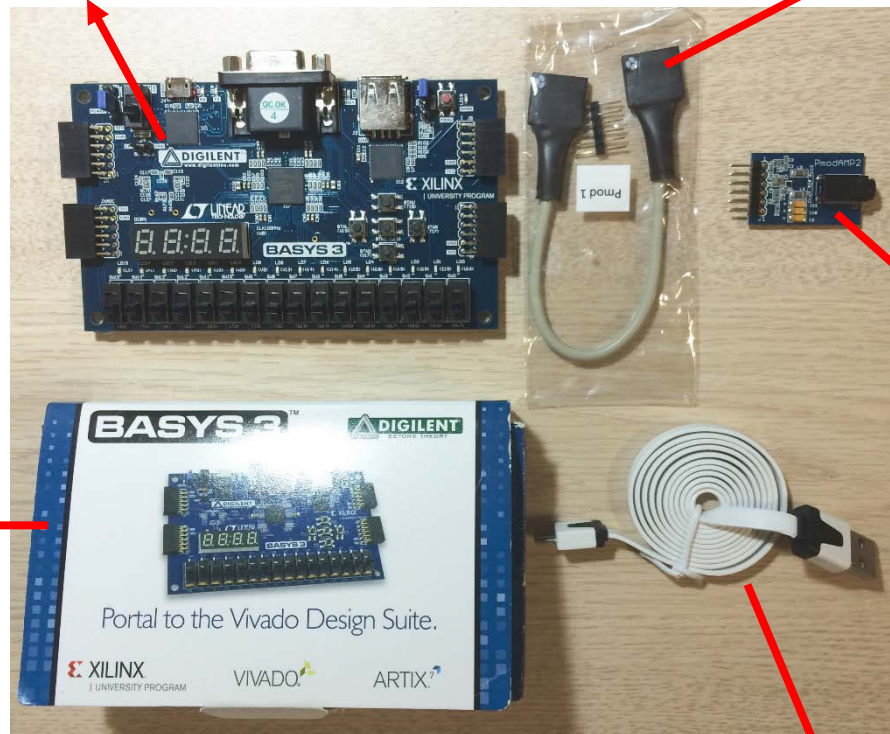
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# FPGA Development Kits



*Basys3* development board

*Pmod* cable

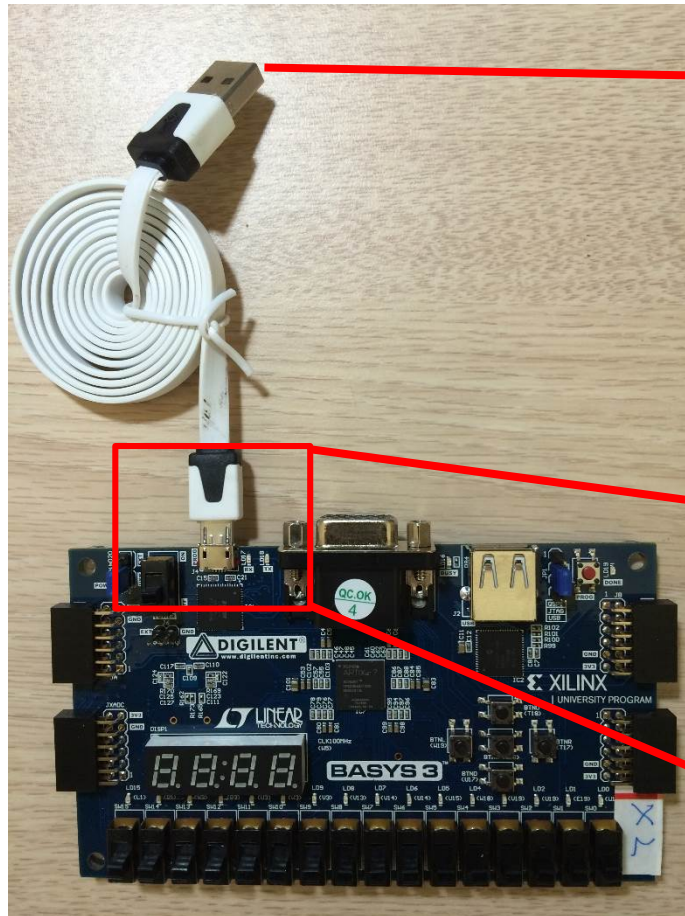


*PmodAMP2*  
audio amplifier

Box

USB-to-microUSB cable

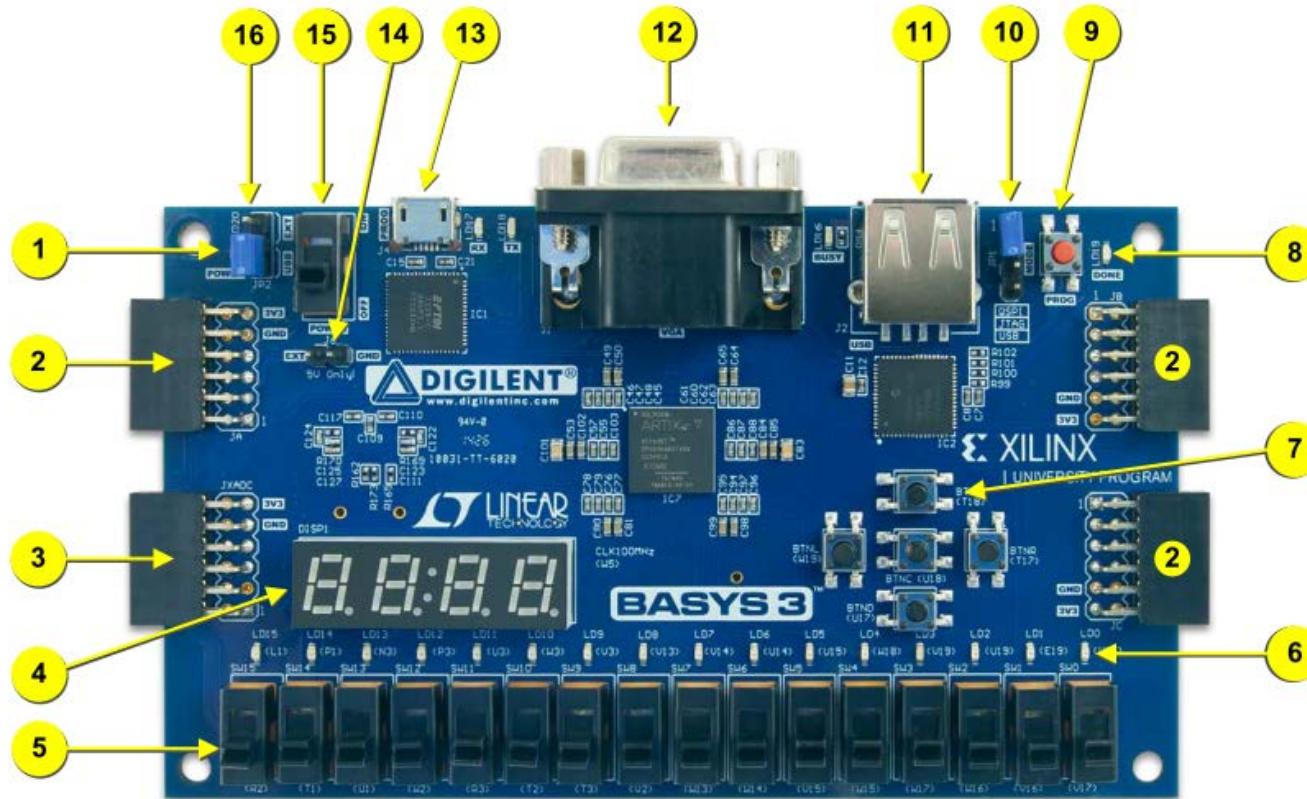
# FPGA Development Kits



Only 5V DC



# Basys3 Demo Board



Callout	Component Description
1	Power good LED
2	Pmod connector(s)
3	Analog signal Pmod connector (XADC)
4	Four digit 7-segment display
5	Slide switches (16)
6	LEDs (16)
7	Pushbuttons (5)
8	FPGA programming done LED
9	FPGA configuration reset button
10	Programming mode jumper
11	USB host connector
12	VGA connector
13	Shared UART/ JTAG USB port
14	External power connector
15	Power Switch
16	Power Select Jumper

Figure 1. Basys3 FPGA board with callouts.



# Create New Project (1/4)



Click this icon



The "Quick Start" sidebar is shown on the left. It contains three main sections: "Quick Start" with buttons for "Create Project &gt;", "Open Project &gt;", and "Open Example Project &gt;"; "Tasks" with buttons for "Manage IP &gt;", "Open Hardware Manager &gt;", and "Xilinx Tcl Store &gt;"; and "Learning Center" with a button for "Documentation and Tutorials &gt;". A red box highlights the "Create Project &gt;" button, and a red arrow points from it to the "Next &gt;" button in the wizard.

The "New Project" wizard dialog is shown on the right. It has a title bar "New Project" and a close button. The main content area is titled "Create a New Vivado Project" and contains the text: "This wizard will guide you through the creation of a new project. To create a Vivado project you will need to provide a name and a location for your project files. Next, you will specify the type of flow you'll be working with. Finally, you will specify your project sources and choose a default part." At the bottom, there is a navigation bar with a help icon, a "&lt; Back" button, a "Next &gt;" button (highlighted with a red box), an "Finish" button, and a "Cancel" button. A red arrow points from the "Create Project" button in the sidebar to the "Next &gt;" button.

# Create New Project (2/4)



- Fill in *project name* and *location*

The screenshot shows a 'New Project' dialog box with the following fields and options:

- Project Name:** A text input field containing 'project\_1', which is highlighted with a red rectangular box.
- Project location:** A text input field containing 'D:/FPGA\_LAB', with a blue border and a red arrow pointing from the 'Project name' field to the 'Next >' button.
- Create project subdirectory
- Project will be created at: D:/FPGA\_LAB/project\_1

At the bottom of the dialog, there are four buttons: a help button (question mark), '< Back', 'Next >' (highlighted in blue), 'Finish', and 'Cancel'.

# Create New Project (3/4)



- Choose *project type*

New Project

**Project Type**

Specify the type of project to create.

**RTL Project**  
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.  
 Do not specify sources at this time

**Post-synthesis Project**  
You will be able to add sources, view device resources, run design analysis, planning and implementation.  
 Do not specify sources at this time

**I/O Planning Project**  
Do not specify design sources. You will be able to view part/package resources.

**Imported Project**  
Create a Vivado project from a Synplify, XST or ISE Project File.

**Example Project**  
Create a new Vivado project from a predefined template.

? < Back Next > Finish Cancel

# Create New Project (4/4)



Find these information on your box

New Project

Default Part

Choose a default Xilinx part or board for your project.

Parts | Boards

Reset All Filters

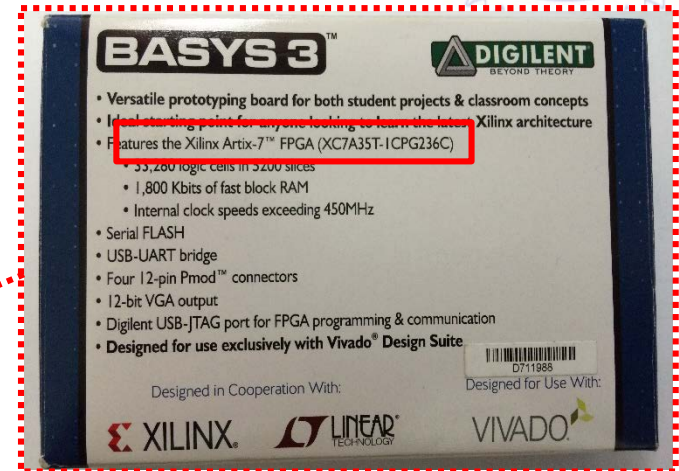
Category: All Package: cpg236 Temperature: All Remaining

Family: Artix-7 Speed: -1 Static power: All Remaining

Search: Q-

Part	I/O Pin Count	Available IOBs	LUT Elements	FlipFlops	Block RAMs	Ultra RAMs	DSPs	Gb Tran
xc7a15tcp236-1	236	106	10400	20800	25	0	45	2
xc7a35tcp236-1	236	106	20800	41600	50	0	90	2
xc7a50tcp236-1	236	106	32600	65200	75	0	120	2

< Back Next > Finish Cancel



New Project Summary

VIVADO

- A new RTL project named 'project\_5' will be created.
- No source files or directories will be added. Use Add Sources to add them later.
- No Configurable IP files will be added. Use Add Sources to add them later.
- No constraints files will be added. Use Add Sources to add them later.

The default part and product family for the new project:  
Default Part: xc7a35tcp236-1  
Product: Artix-7  
Family: Artix-7  
Package: cpg236  
Speed Grade: -1

To create the project, click Finish

Finish Cancel





# Simulation (1/4): Add Source

- Add sources (e.g., design, testbench, ...etc)

The screenshot shows the Vivado 2019.2 interface. The 'Add Sources' dialog box is open, displaying the following options:

- Add or create constraints
- Add or create design sources
- Add or create simulation sources

The 'Next >' button is highlighted with a red arrow. The background shows the 'PROJECT MANAGER' window with the 'Add Sources' button highlighted in the left sidebar.

指定和或创建源文件添加到工程

# Simulation (2/4): Add Source



The screenshot shows the 'Add Sources' dialog in Xilinx Vivado. The main window is titled 'Add Sources' and contains the following elements:

- Add or Create Design Sources:** A section with instructions: 'Specify HDL, netlist, Block Design, and IP files, or directories containing those file types to add to your project. Create a new source file on disk and add it to your project.'
- Table:** A table listing the added sources. A red box highlights the first two rows, and a red arrow points from the text 'Your design and corresponding testbench' to this table.
- Buttons:** 'Add Files', 'Add Directories', and 'Create File' buttons are visible. A red arrow points from the table to the 'Add Files' button.
- Checkboxes:** 'Scan and add RTL include files into project', 'Copy sources into project', and 'Add sources from subdirectories' (checked).
- Navigation:** '< Back', 'Next >', 'Finish', and 'Cancel' buttons. A red arrow points from the table to the 'Finish' button.
- File Selection:** A 'Look in:' field shows 'CODE'. Below it, a list of files includes 'binup\_counter.v' and 'binup\_counter\_tb.v', which are highlighted with a red box. A red arrow points from this box to the 'OK' button at the bottom.
- File Name and Type:** 'File name:' and 'Files of type:' fields are visible at the bottom.

Index	Name	Library	Location
1	binup_counter.v	xil_defaultlib	C:/Users/LAB_626/Desktop/CODE
2	binup_counter_tb.v	xil_defaultlib	C:/Users/LAB_626/Desktop/CODE



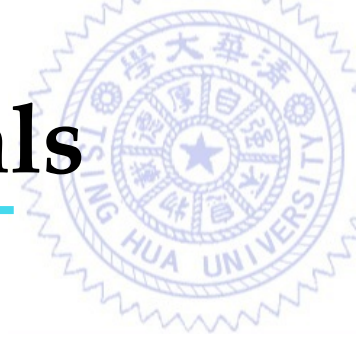
# Simulation (3/4): Run Simulation

- *Run Simulation -> Run behavioral Simulation*

The screenshot shows the Vivado 2019.2 interface. The 'Run Simulation' menu is open, and 'Run Behavioral Simulation' is highlighted. The 'Project Manager' window shows the project 'project\_1' with sources including 'binup\_counter\_tb'. The 'Project Summary' window shows project details like 'Project name: project\_1', 'Project location: D:/FPGA\_LAB/project\_1', and 'Product family: Artix-7'. The 'Design Runs' table is visible at the bottom.

Run	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy	Rep
synth_1	constrs_1	Not started													Vivado Synthesis Defaults (Vivado Synthesis 2019)	Viva
impl_1	constrs_1	Not started													Vivado Implementation Defaults (Vivado Implementation 2019)	Viva

# Simulation (4/4): Check Signals



- Show waveform

The screenshot displays the Vivado 2019.2 simulation environment. The main window shows a behavioral simulation of a counter circuit. The 'Scope' pane on the left lists the design elements: binup\_cou, binup\_cou, and gbl. The 'Objects' pane in the center shows the current state of the simulation: clk is 1, rst is 0, and q[3] is f. The waveform window on the right shows the signal values over time, with a yellow vertical line indicating the current simulation time at 210,000 ps. The Tcl Console at the bottom shows the simulation results, including the completion of the synthesis and the simulation run for 1000ns.

Name	Value	209,995 ps	209,996 ps	209,997 ps	209,998 ps	209,999 ps	210,000 ps
clk	1						
rst	0						
q[3:0]	f						

```
INFO: [USF-XSim-96] XSim completed. Design snapshot 'binup_counter_tb_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:12 ; elapsed = 00:00:24 . Memory (MB): peak = 838.277 ; gain = 0.000
```

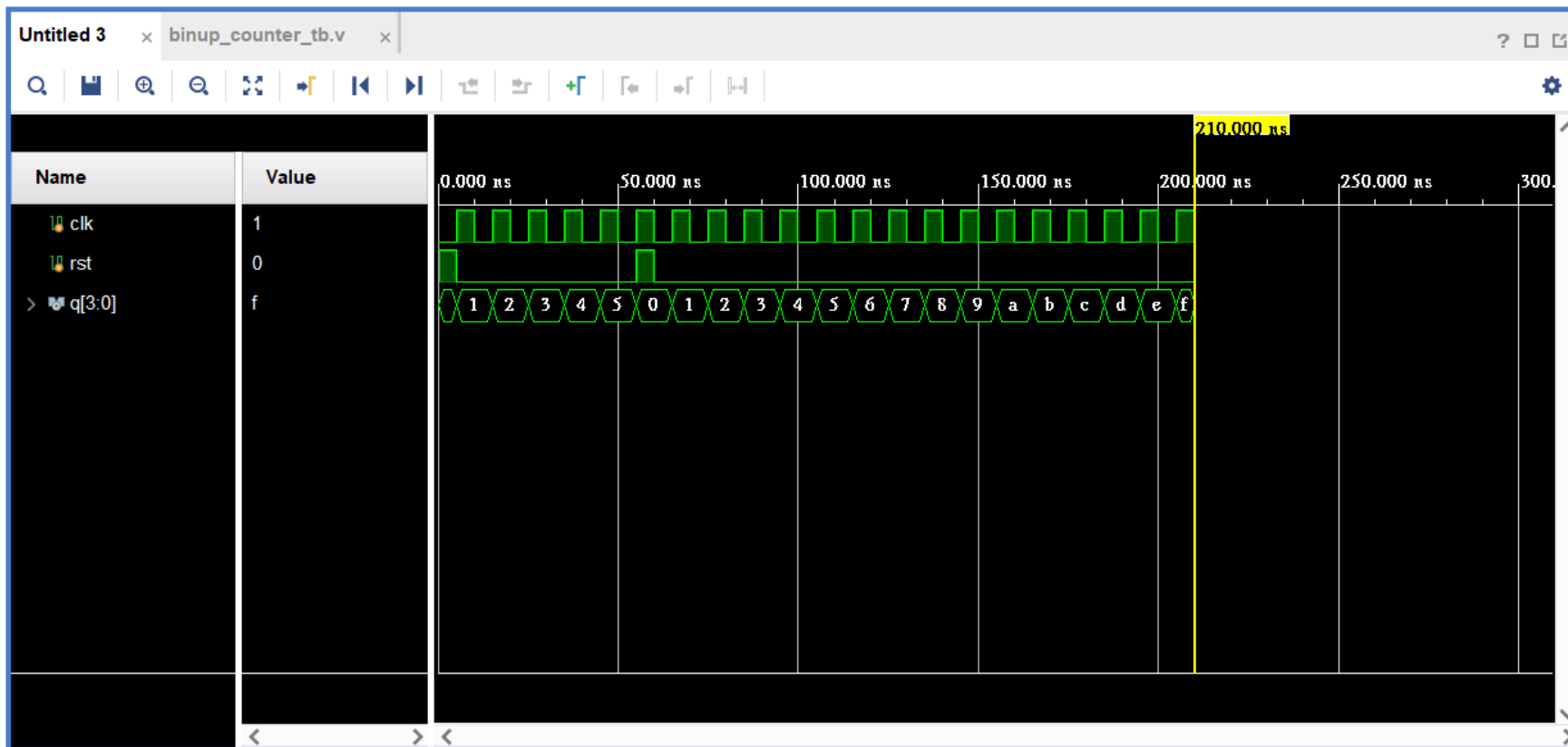
# Debugging The Design (1/4)



- Zoom fit



Unfit waveform





# Debugging The Design (2/4)



- Reorder the signals

Choose the *block* that you want to see

The screenshot shows a logic simulator interface with three main panels:

- Block Diagram:** Shows a hierarchy of components. The `binup_counter` block is highlighted with a red box. A red arrow points from the text "Choose the block that you want to see" to this block.
- Object Table:** A table listing the selected object and its properties.
- Waveform:** A timing diagram showing signals over time. A vertical yellow cursor is at 210,000 ns. Three red arrows point to the signals: `clk`, `rst`, and `q[3:0]`.

Name	Value	Data
clk	1	Lo
rst	0	Lo
q[3:0]	f	Ar
q_temp[3:0]	0	Ar

Name	Value
clk	1
rst	0
q[3:0]	f

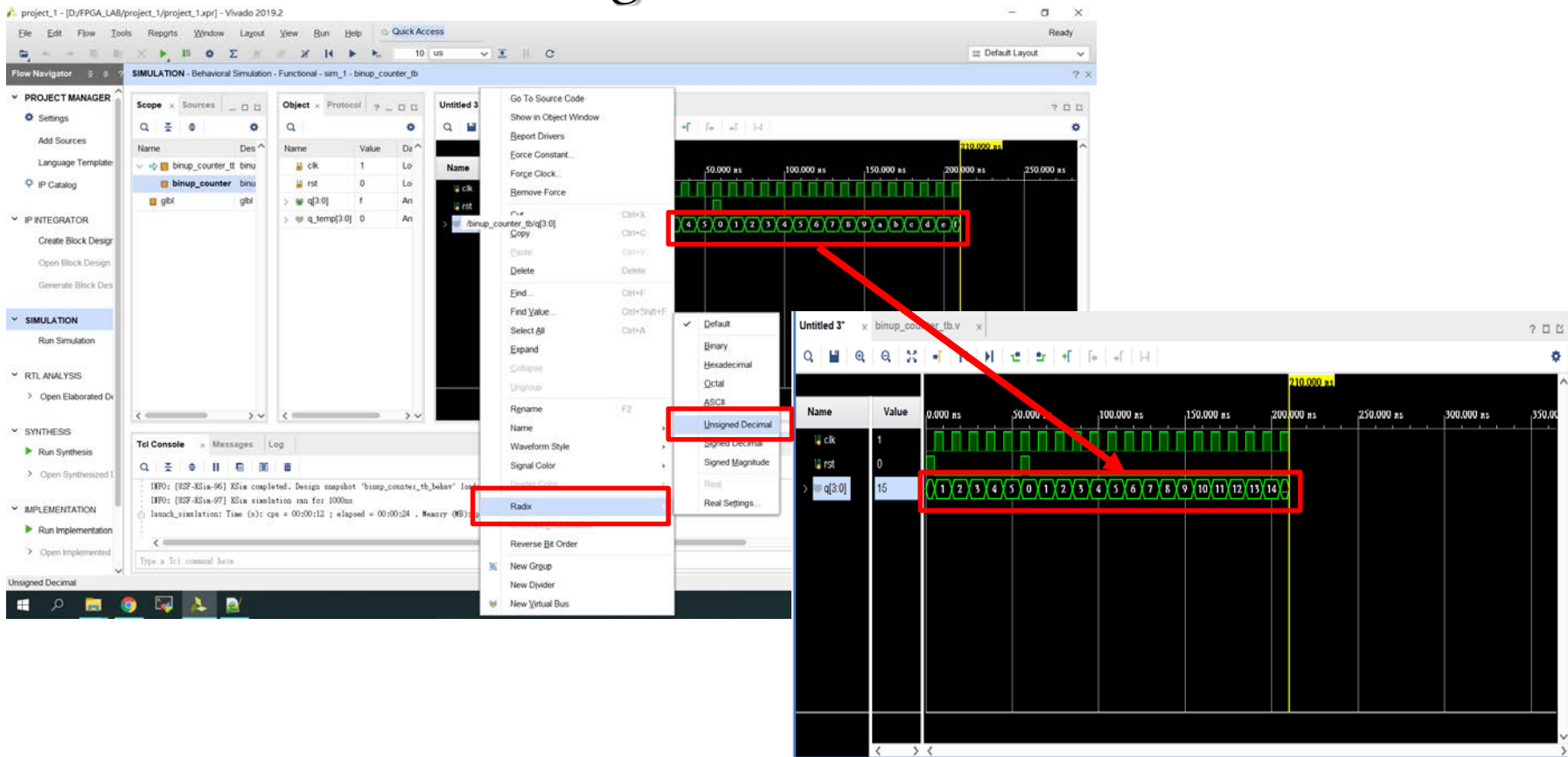
Waveform signals: `clk`, `rst`, `q[3:0]`

1. clock
2. Inputs
3. output



# Debugging The Design (3/4)

- Right click to open the popup menu again, and select *Radix > Unsigned Decimal*



# Debugging The Design (4/4)



- Right click to open the popup menu again, and select *New Divider*

The screenshot shows the Vivado 2019.2 simulation environment. The main window displays a behavioral simulation for a binup\_counter. The waveform shows the clock (clk) and reset (rst) signals, along with the 4-bit output (q[3:0]). A context menu is open over the waveform, with the 'New Divider' option highlighted. The 'New Divider' option is also highlighted in the bottom status bar of the Vivado interface.

Name	Value
clk	0
rst	0
q[3:0]	4
New Divider	

# Reference



- You can find the tutorial of Vivado in *DocNav* (e.g., ug937-vivado-design-suite-simulation-tutorial.pdf)

