EECS 207002
Logic Design Laboratory
邏輯設計實驗

Vivado Simulation

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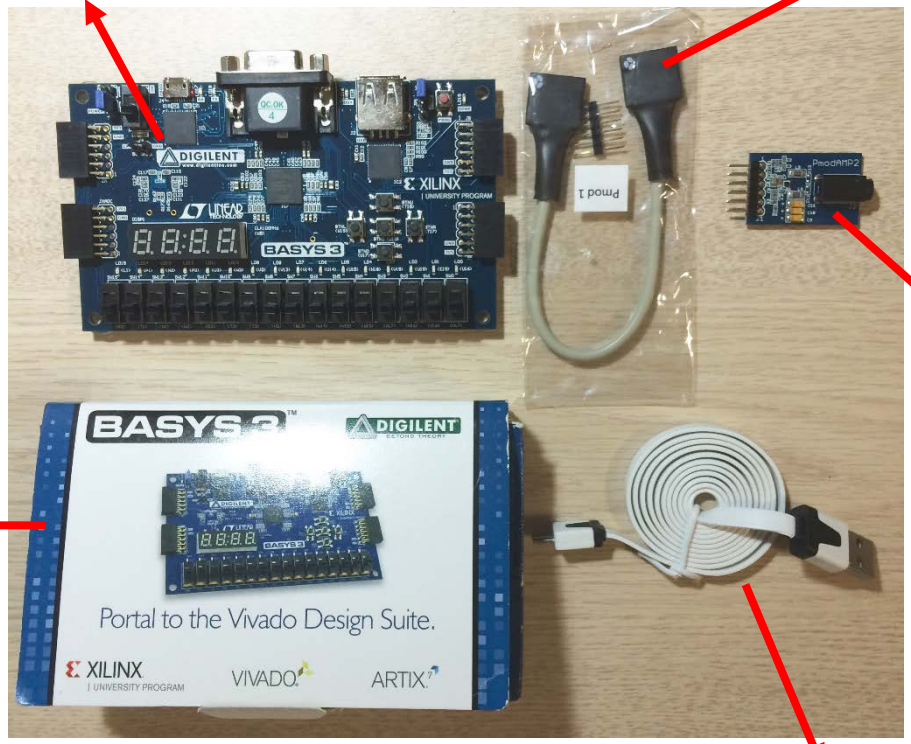
FPGA Development Kits

Basys3 development board

Pmod cable

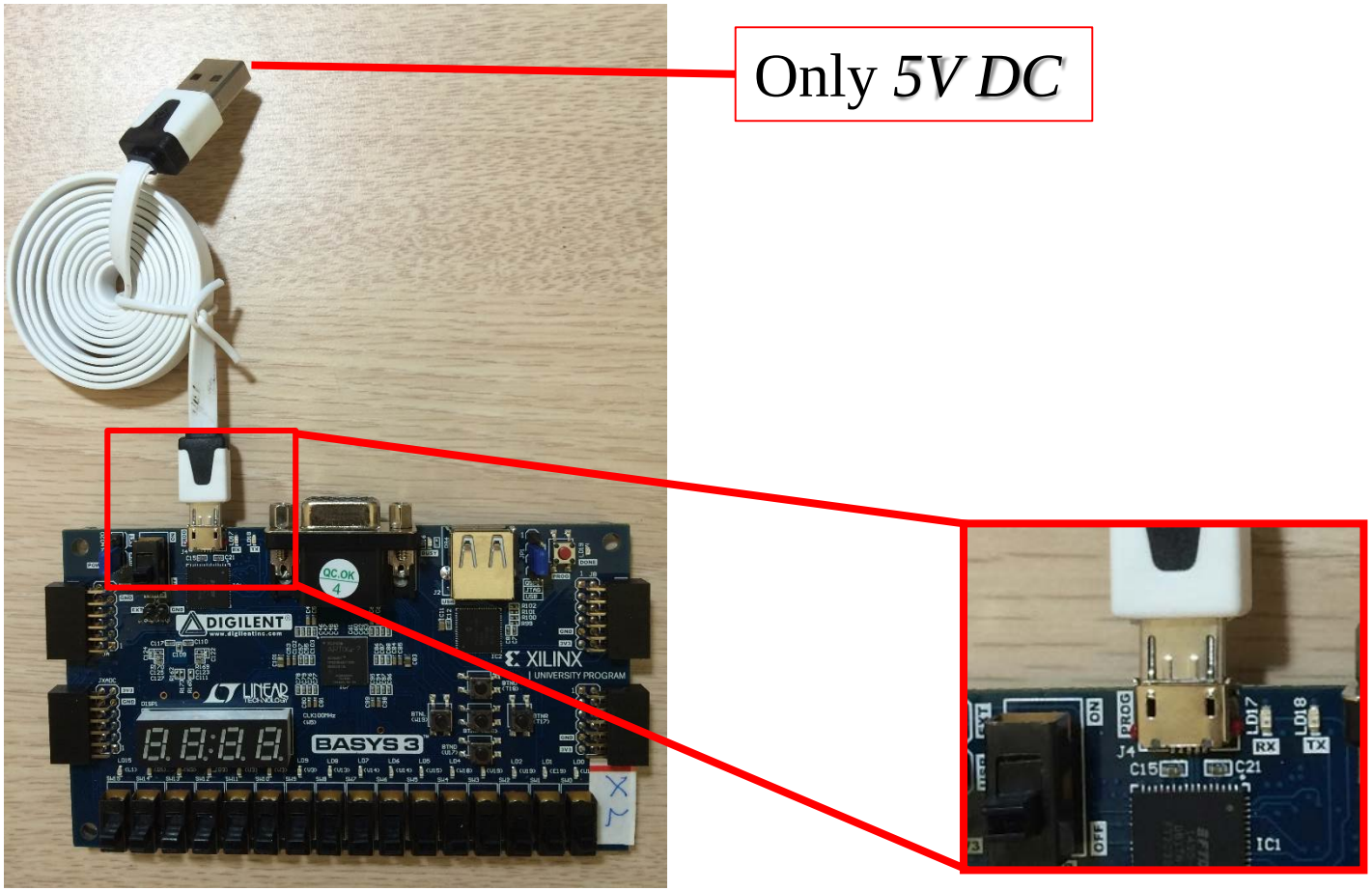


PmodAMP2
audio amplifier

Box

USB-to-microUSB cable

FPGA Development Kits



Basys3 Demo Board

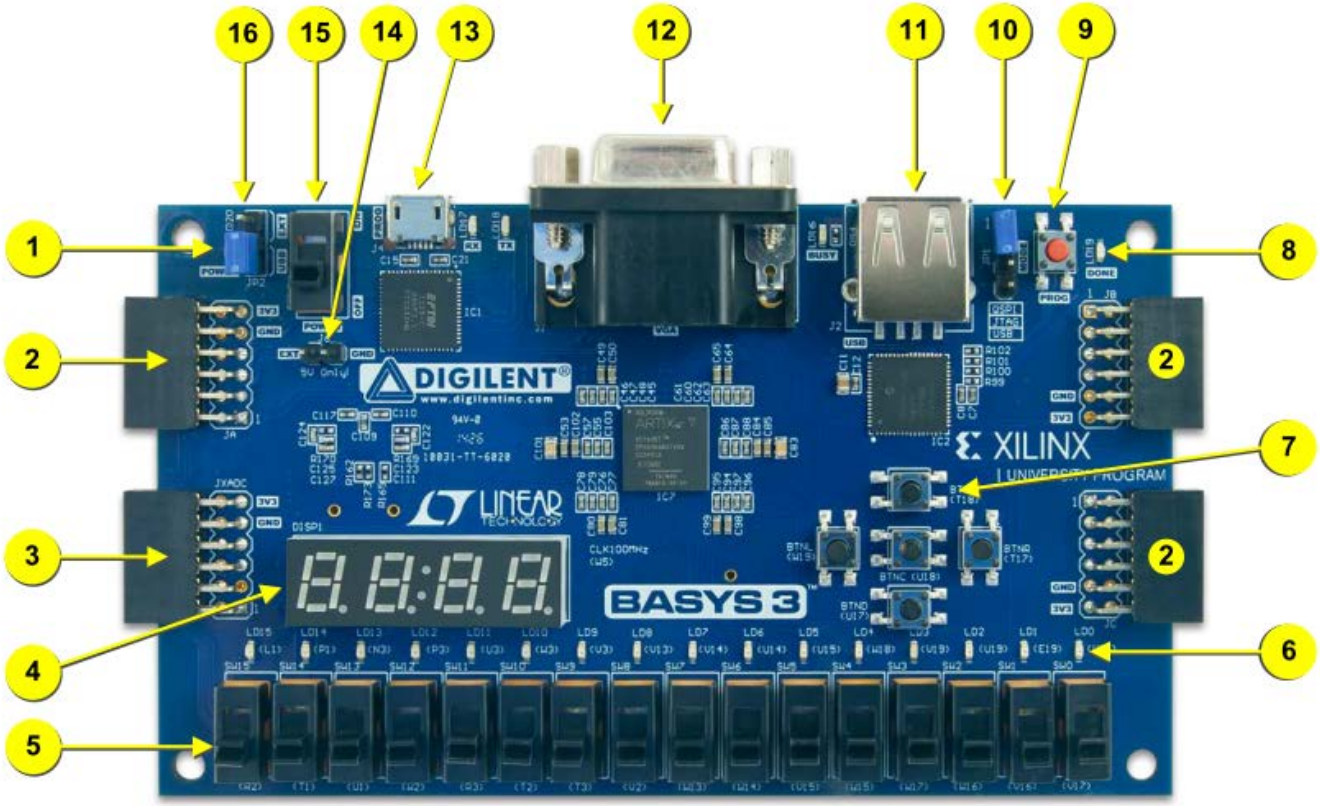
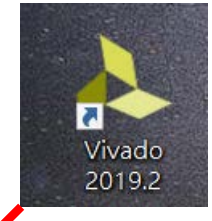


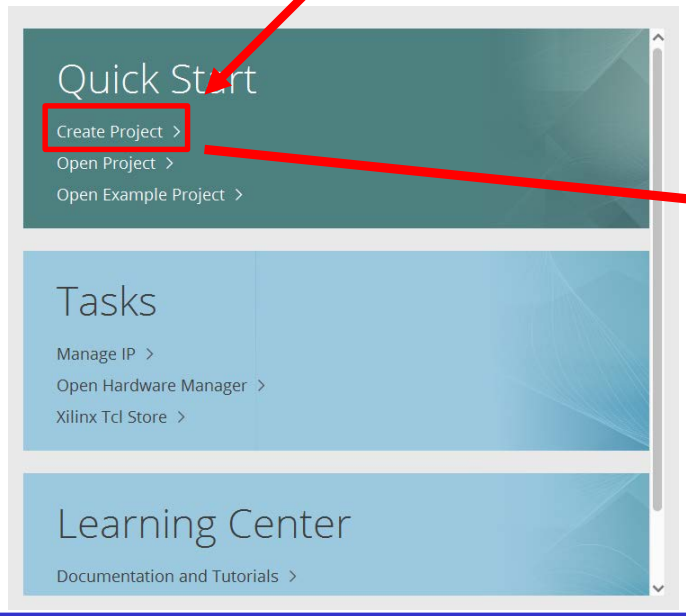
Figure 1. Basys3 FPGA board with callouts.

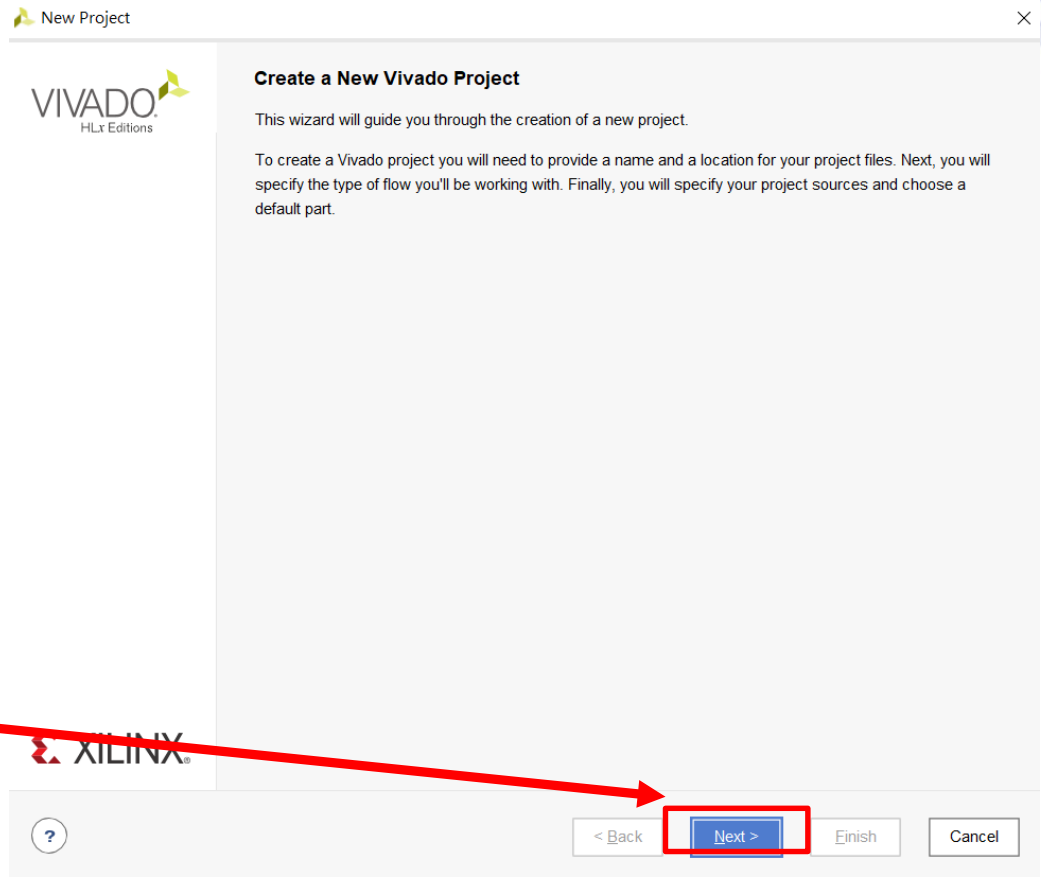
Callout	Component Description
1	Power good LED
2	Pmod connector(s)
3	Analog signal Pmod connector (XADC)
4	Four digit 7-segment display
5	Slide switches (16)
6	LEDs (16)
7	Pushbuttons (5)
8	FPGA programming done LED
9	FPGA configuration reset button
10	Programming mode jumper
11	USB host connector
12	VGA connector
13	Shared UART/ JTAG USB port
14	External power connector
15	Power Switch
16	Power Select Jumper

Create New Project (1/4)

Click this icon

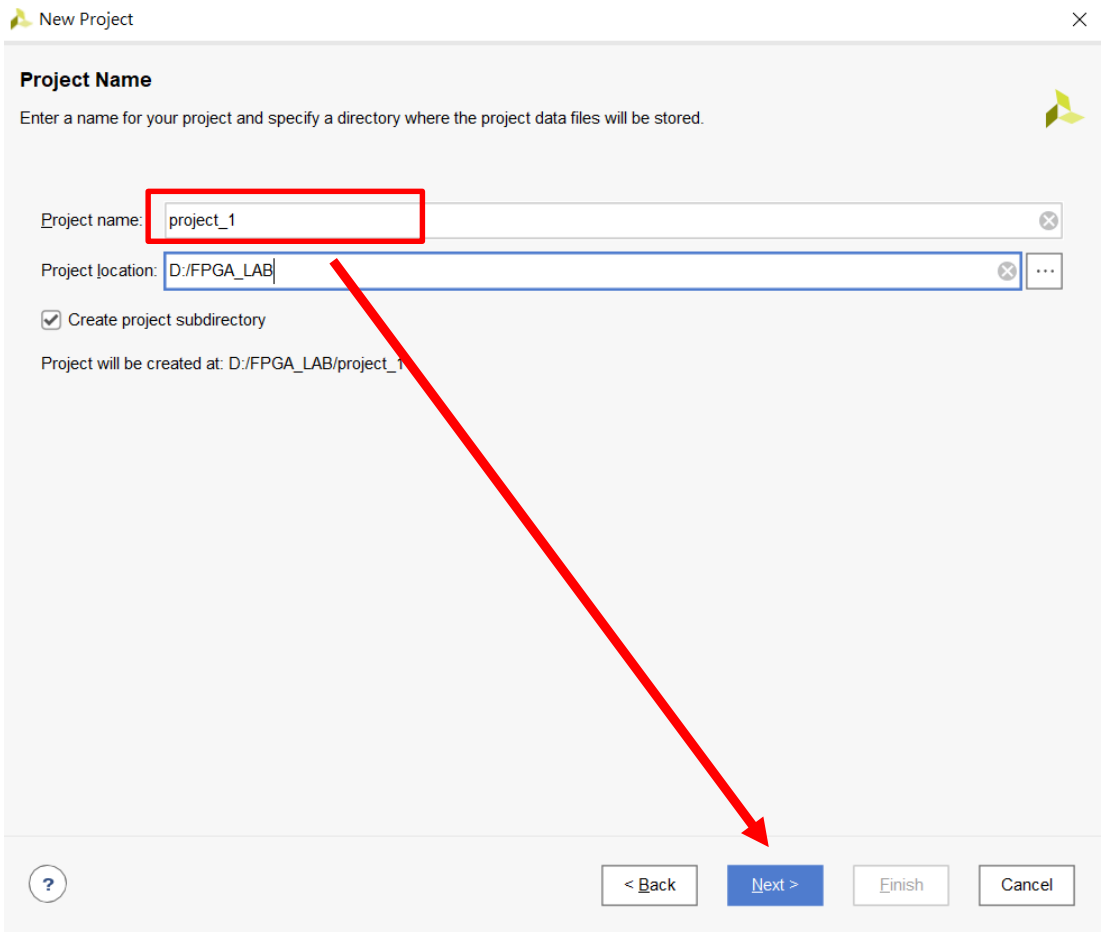






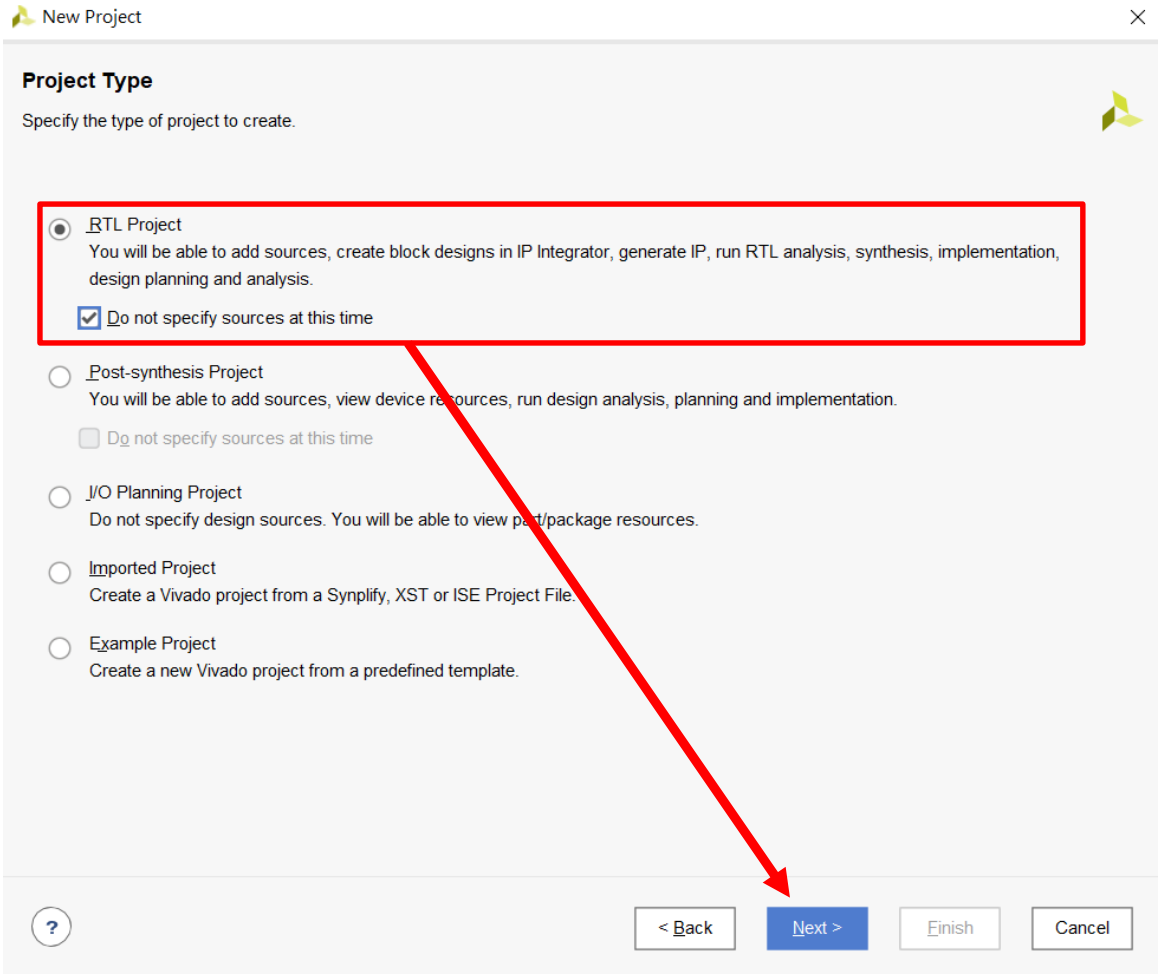
Create New Project (2/4)

- Fill in *project name* and *location*



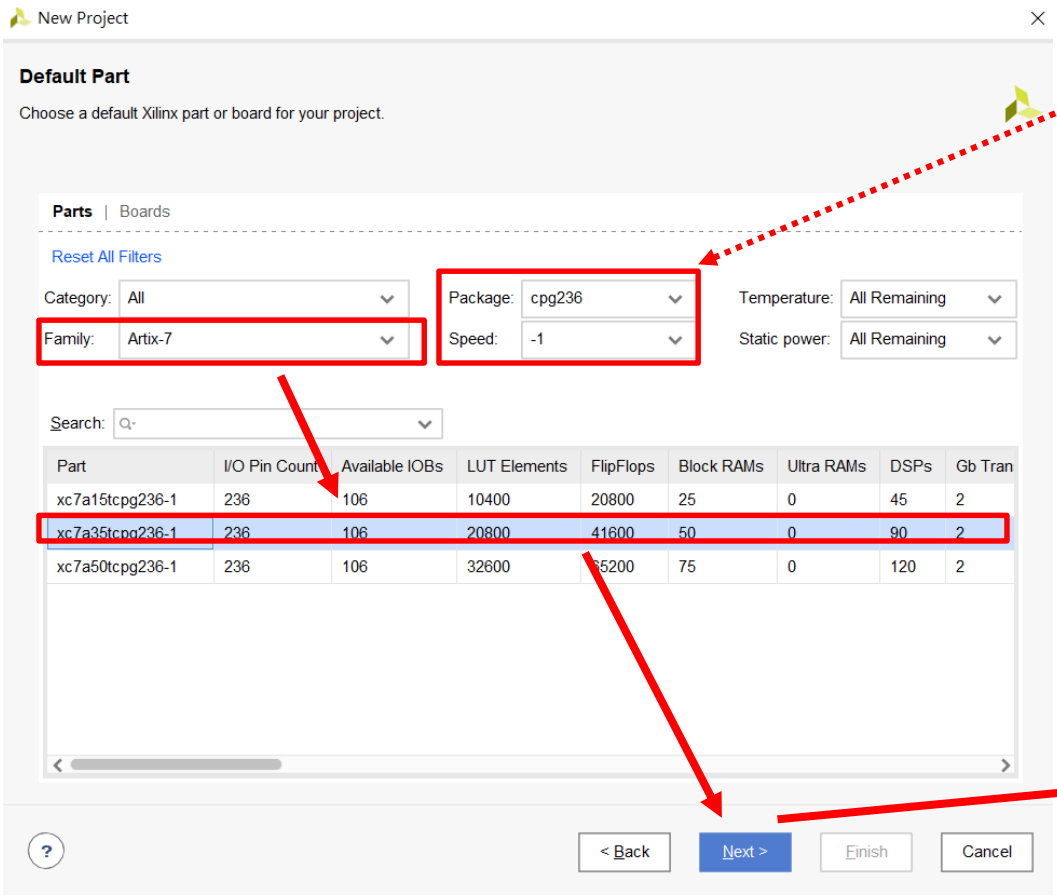
Create New Project (3/4)

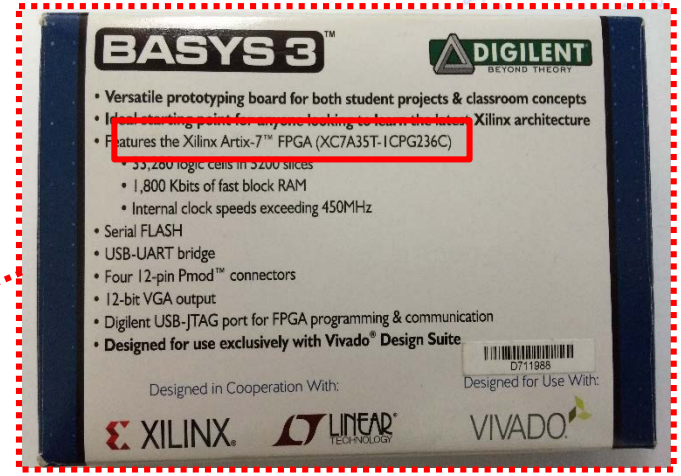
- Choose *project type*

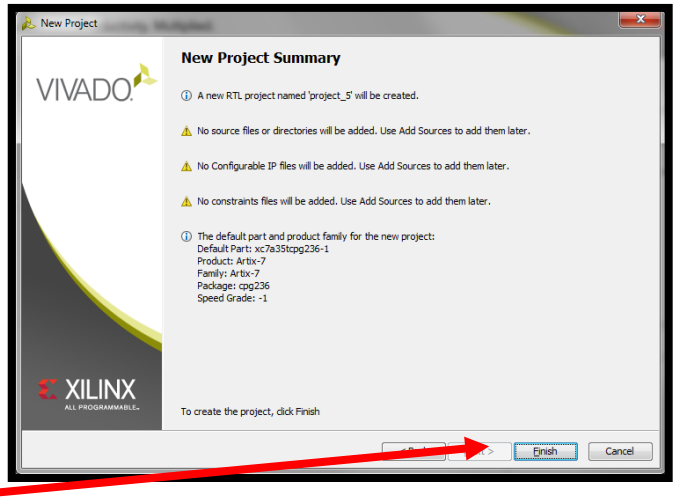


Create New Project (4/4)

Find these information on your box

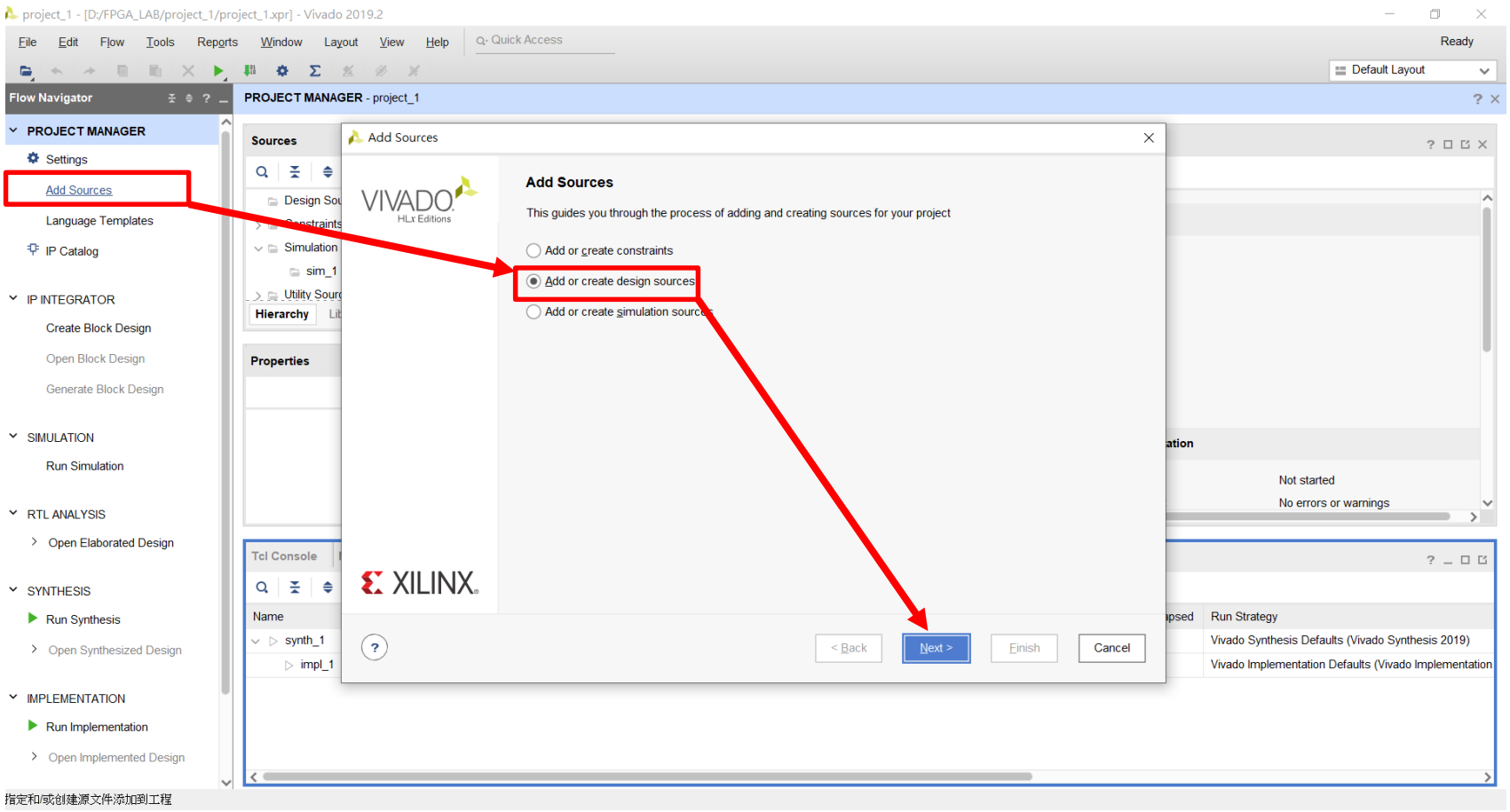




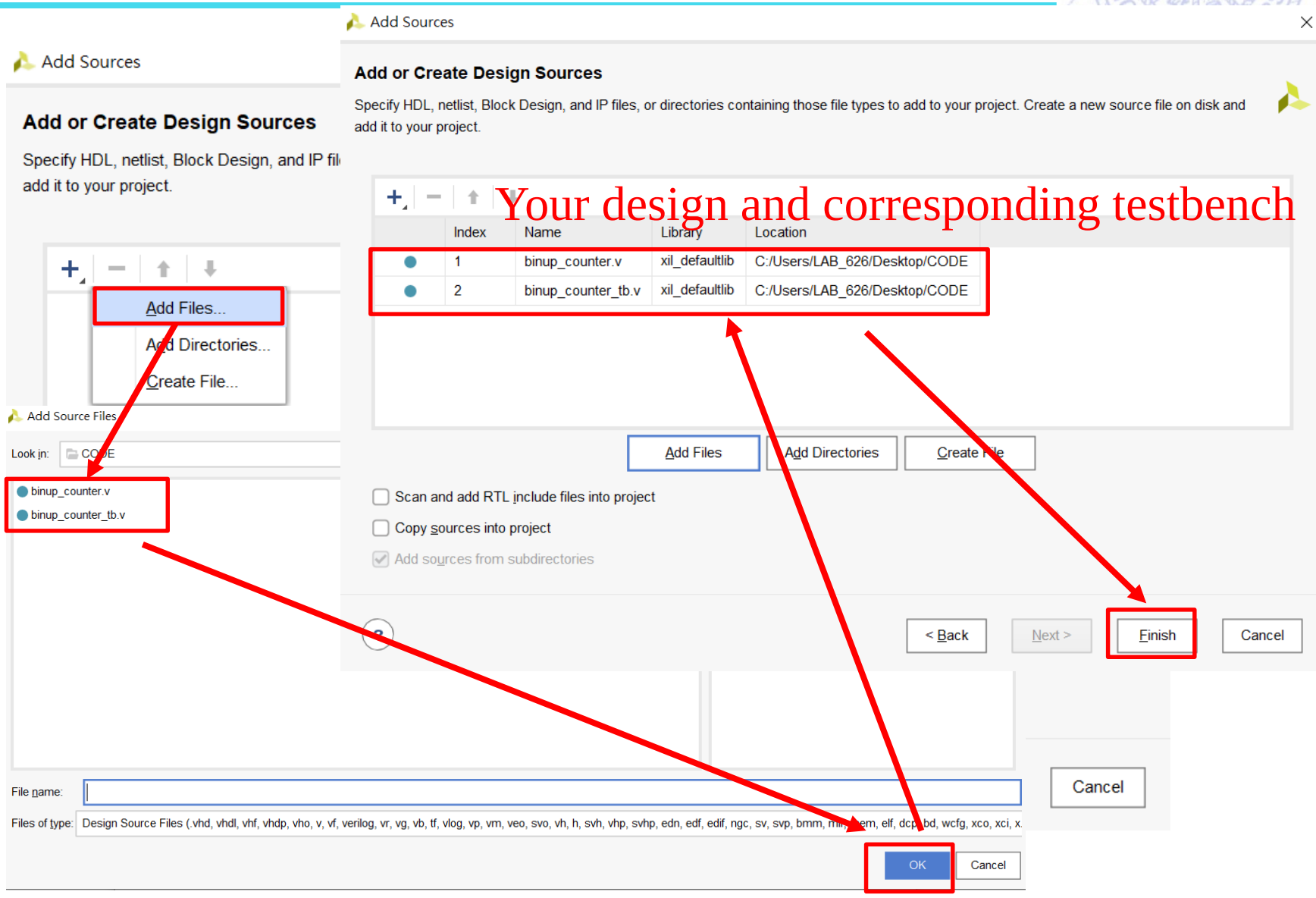


Simulation (1/4): Add Source

- Add sources (e.g., design, testbench, …etc)

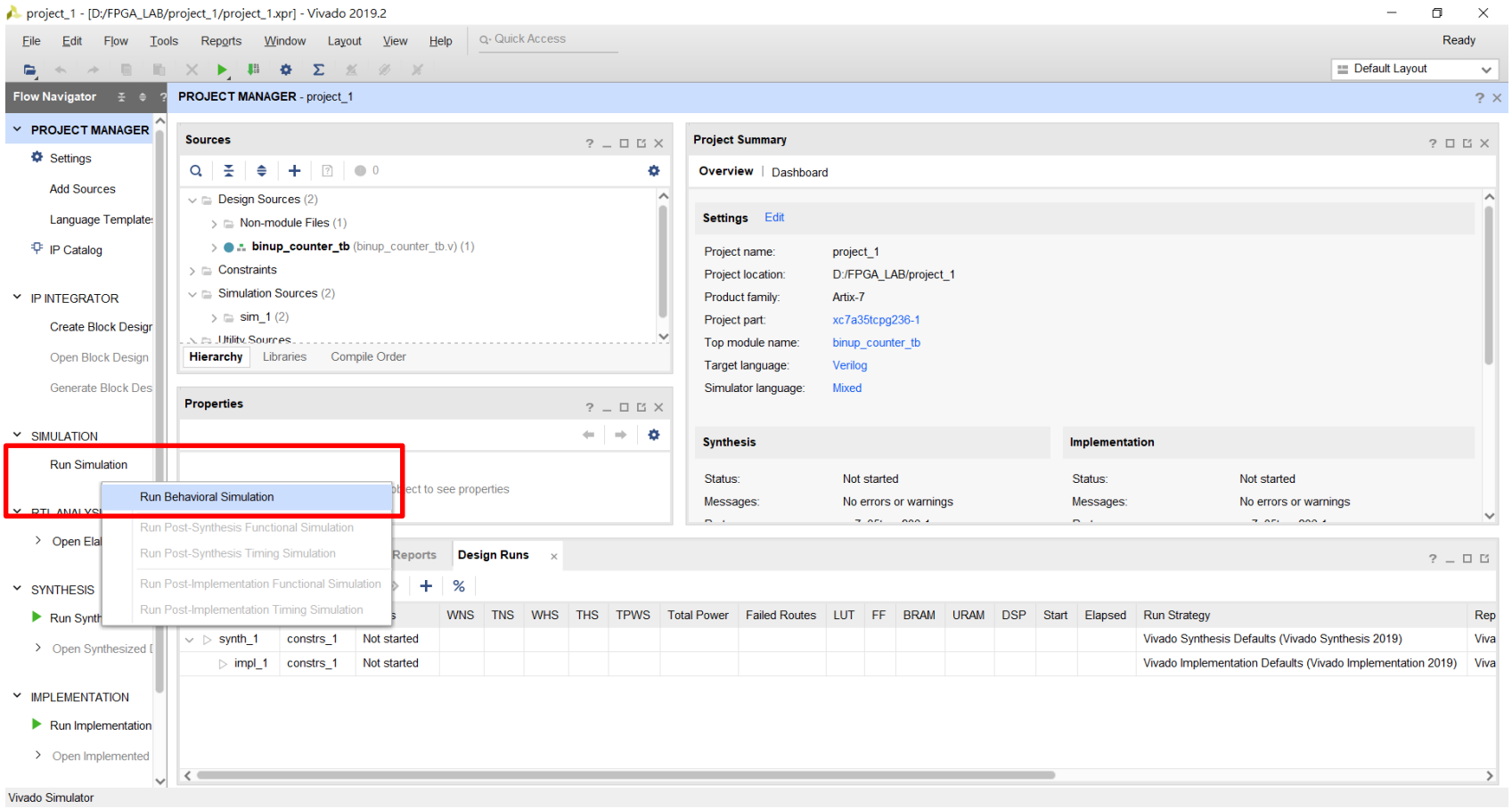


Simulation (2/4): Add Source



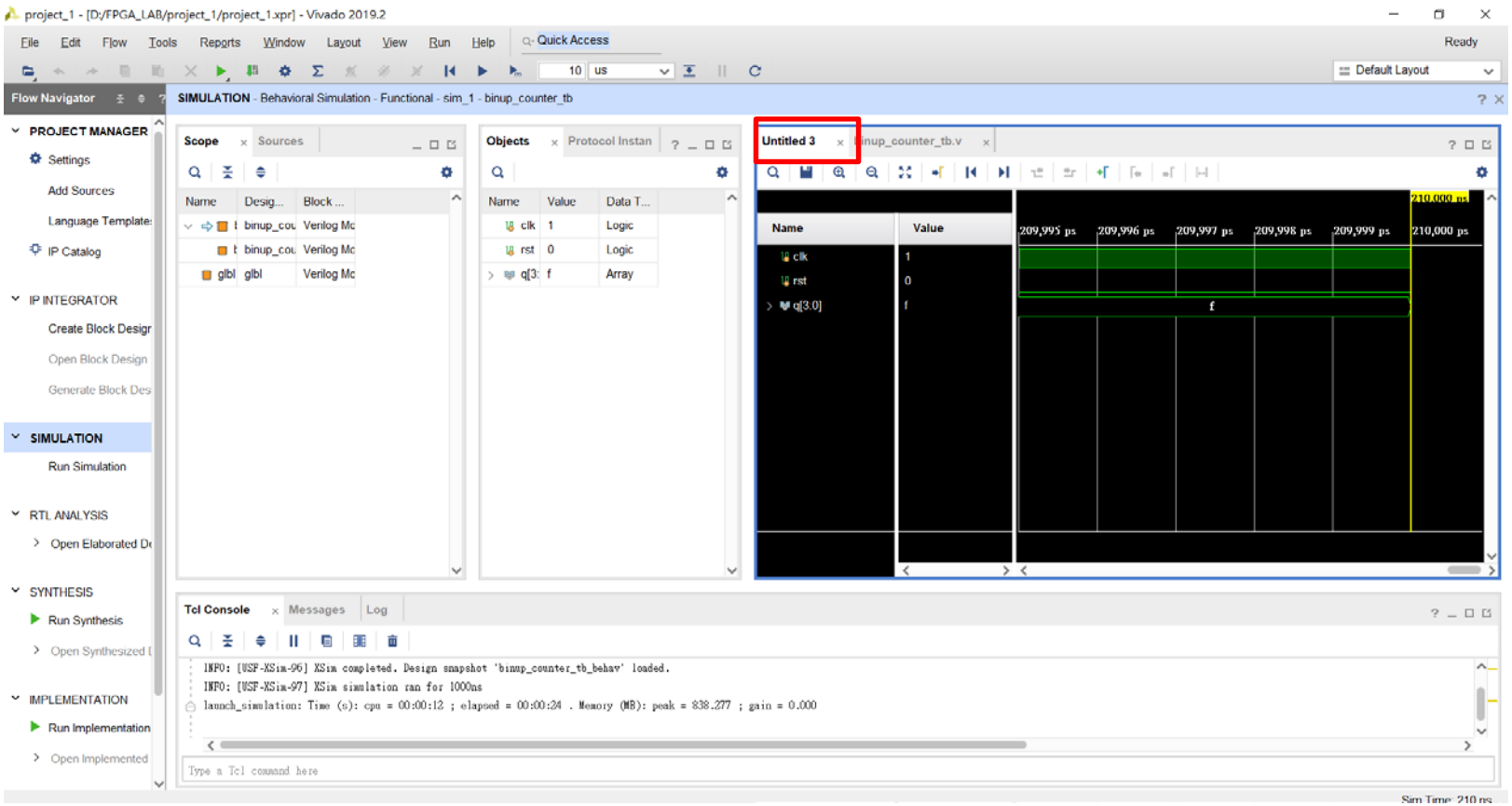
Simulation (3/4): Run Simulation

- *Run Simulation -> Run behavioral Simulation*



Simulation (4/4): Check Signals

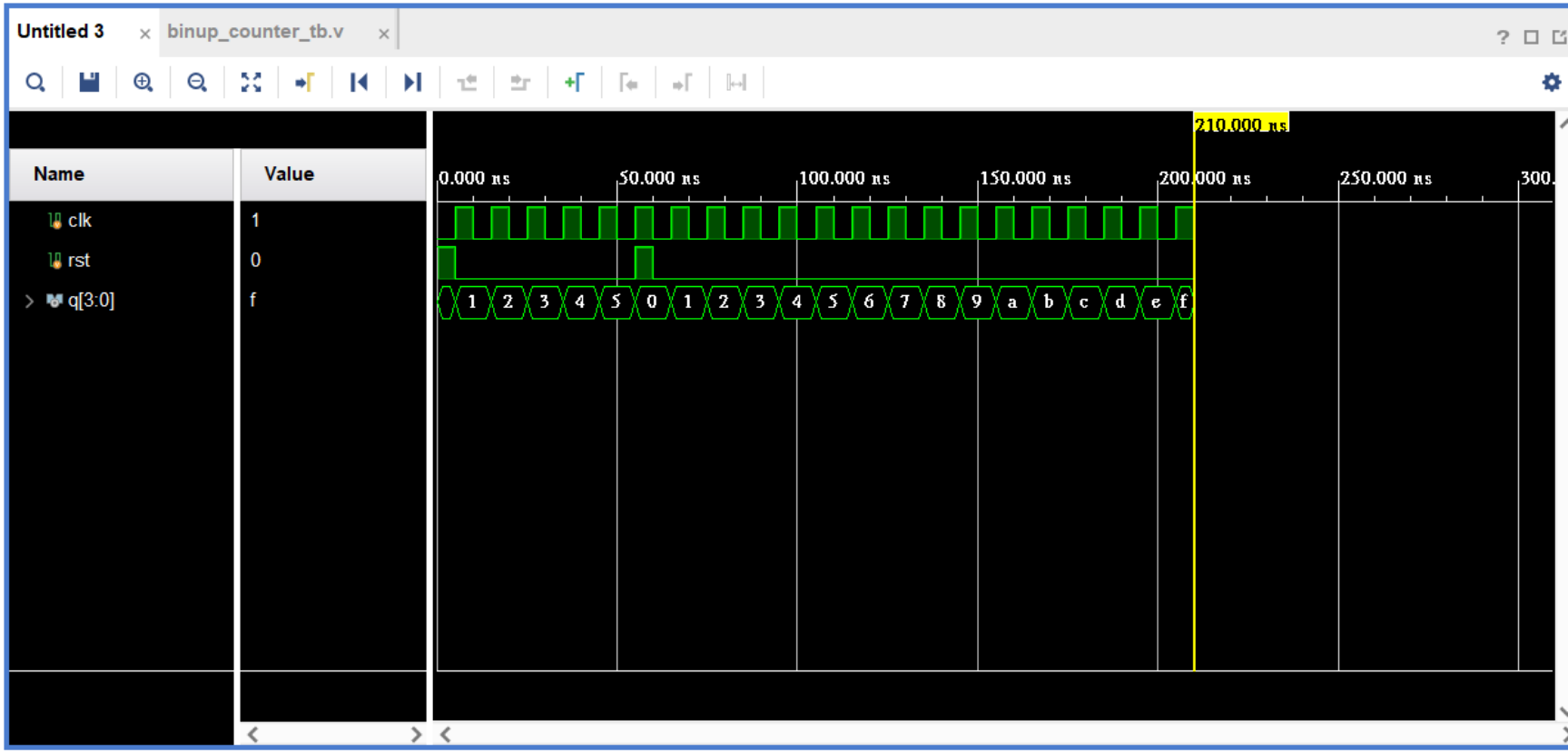
- Show waveform



Debugging The Design (1/4)

- Zoom fit 

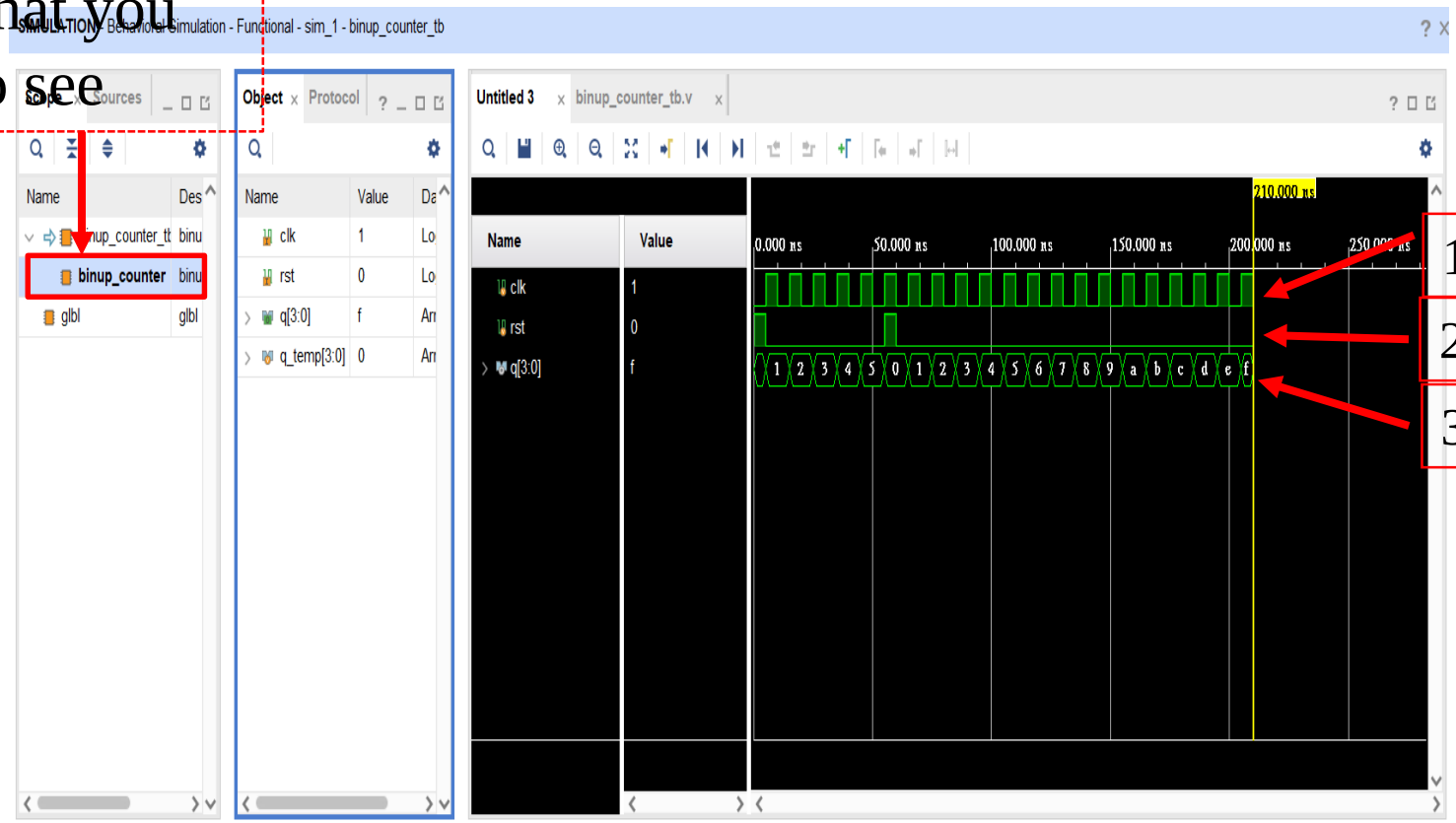
Unfit waveform



Debugging The Design (2/4)

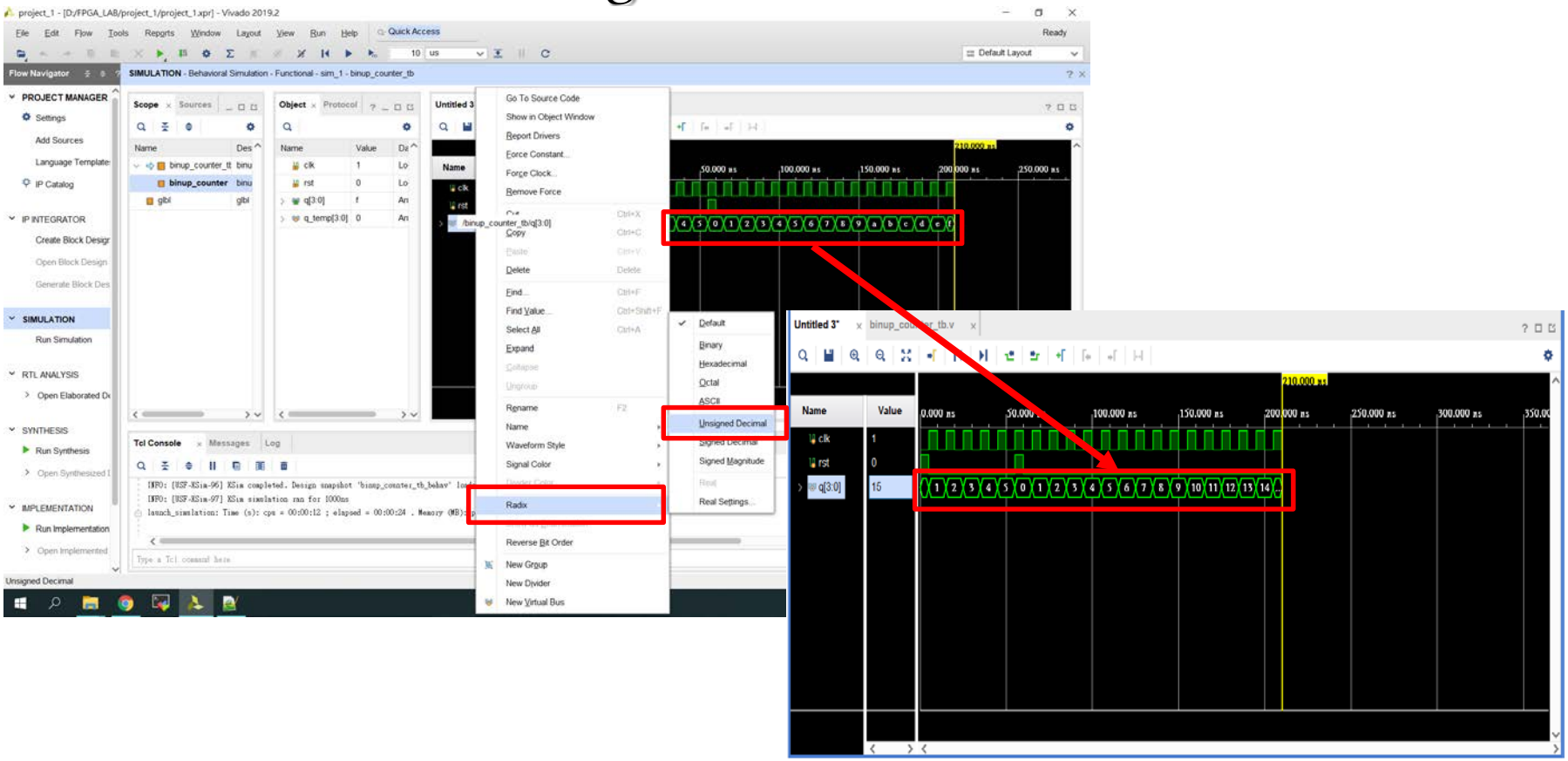
- Reorder the signals

Choose the *block* that you want to see



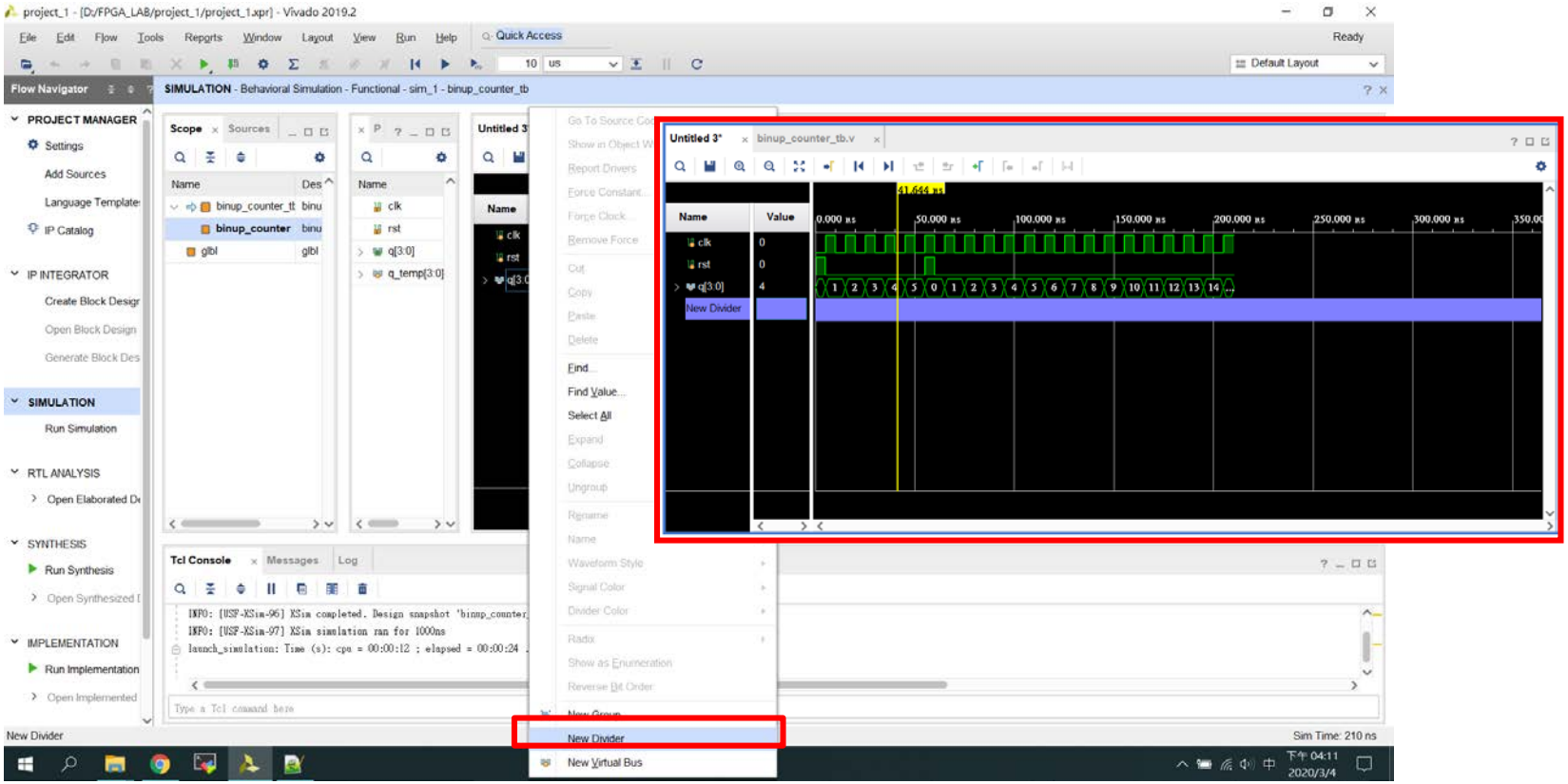
Debugging The Design (3/4)

- Right click to open the popup menu again, and select *Radix* > *Unsigned Decimal*



Debugging The Design (4/4)

- Right click to open the popup menu again, and select *New Divider*



Reference

- You can find the tutorial of Vivado in *DocNav*

(e.g., ug937-vivado-design-suite-simulation-tutorial.pdf)