



FPGA Emulation

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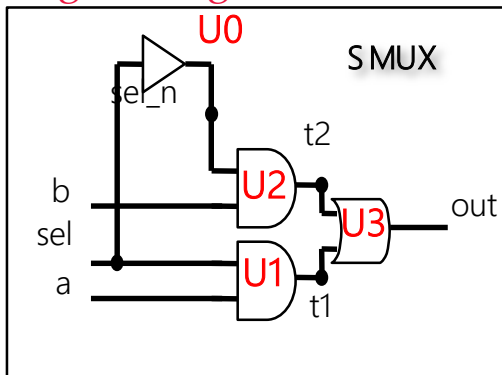
Verilog HDL Utilization Scenario I

- Simulation and verification of logic circuits on PC.

Specification



Logic Design



Verilog HDL Coding

```

module SMUX(out, a, b, sel);
    output out;
    input a,b,sel;
    wire sel_n,t1,t2;

    not U0(sel_n,sel);
    and U1(t1,a,sel);
    and U2(t2,b,sel_n);
    or U3(out,t1,t2);

endmodule

```

Test Pattern

a, b, sel
000
001
010
...
111

Yes, it is correct!



Verilog HDL Simulator

- Imaging what happens when the circuit is as complex as a CPU or MP3 player processor.



Verilog HDL Utilization Scenario II

- Design and Implementation of logic circuits in FPGA (IC)

Specification

2-to-1 Multiplexer

Verilog HDL Coding

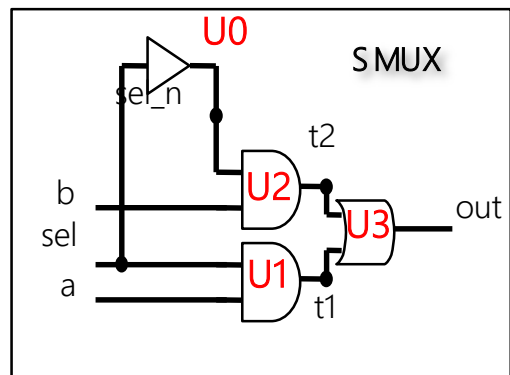
```

module SMUX(out, a, b, sel);
output out;
input a,b,sel;
wire sel_n,t1,t2;

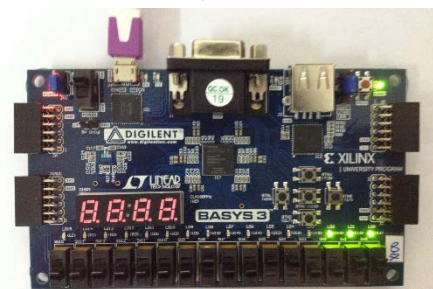
assign out = sel ? a:b;
endmodule

```

Synthesized Logic Circuits



FPGA Implement Design and Programming



Now, it can work !



Verilog HDL Logic Synthesizer



Basys3 FPGA Board

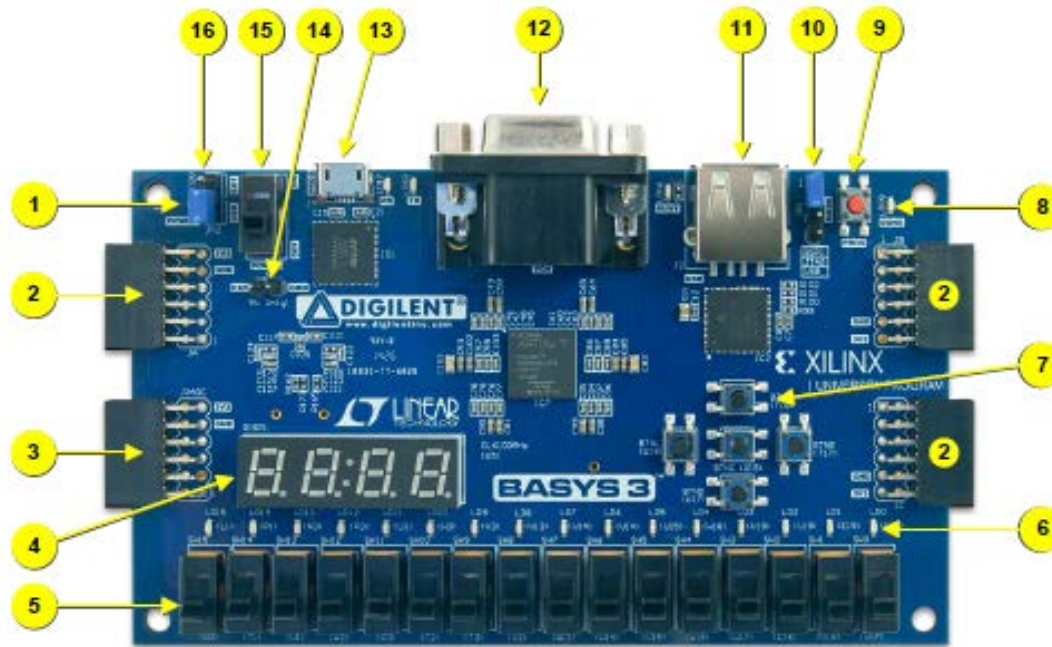
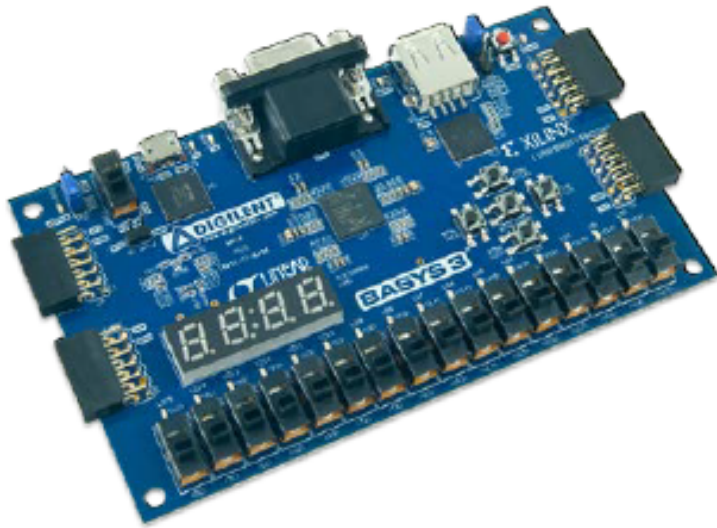


Figure 1. Basys3 FPGA board with callouts.

Callout	Component Description	Callout	Component Description
1	Power good LED	9	FPGA configuration reset button
2	Pmod connector(s)	10	Programming mode jumper
3	Analog signal Pmod connector (XADC)	11	USB host connector
4	Four digit 7-segment display	12	VGA connector
5	Slide switches (16)	13	Shared UART/ JTAG USB port
6	LEDs (16)	14	External power connector
7	Pushbuttons (5)	15	Power Switch
8	FPGA programming done LED	16	Power Select Jumper

Table 1. Basys3 Callouts and component descriptions.

EVS6 FPGA Board Specification



- 33,280 logic cells in 5200 slices (each slice contains four 6-input LUTs and 8 flip-flops)
- 1,800 Kbits of fast block RAM
- Five clock management tiles, each with a phase-locked loop (PLL)
- 90 DSP slices
- Internal clock speeds exceeding 450MHz
- On-chip analog-to-digital converter (XADC)

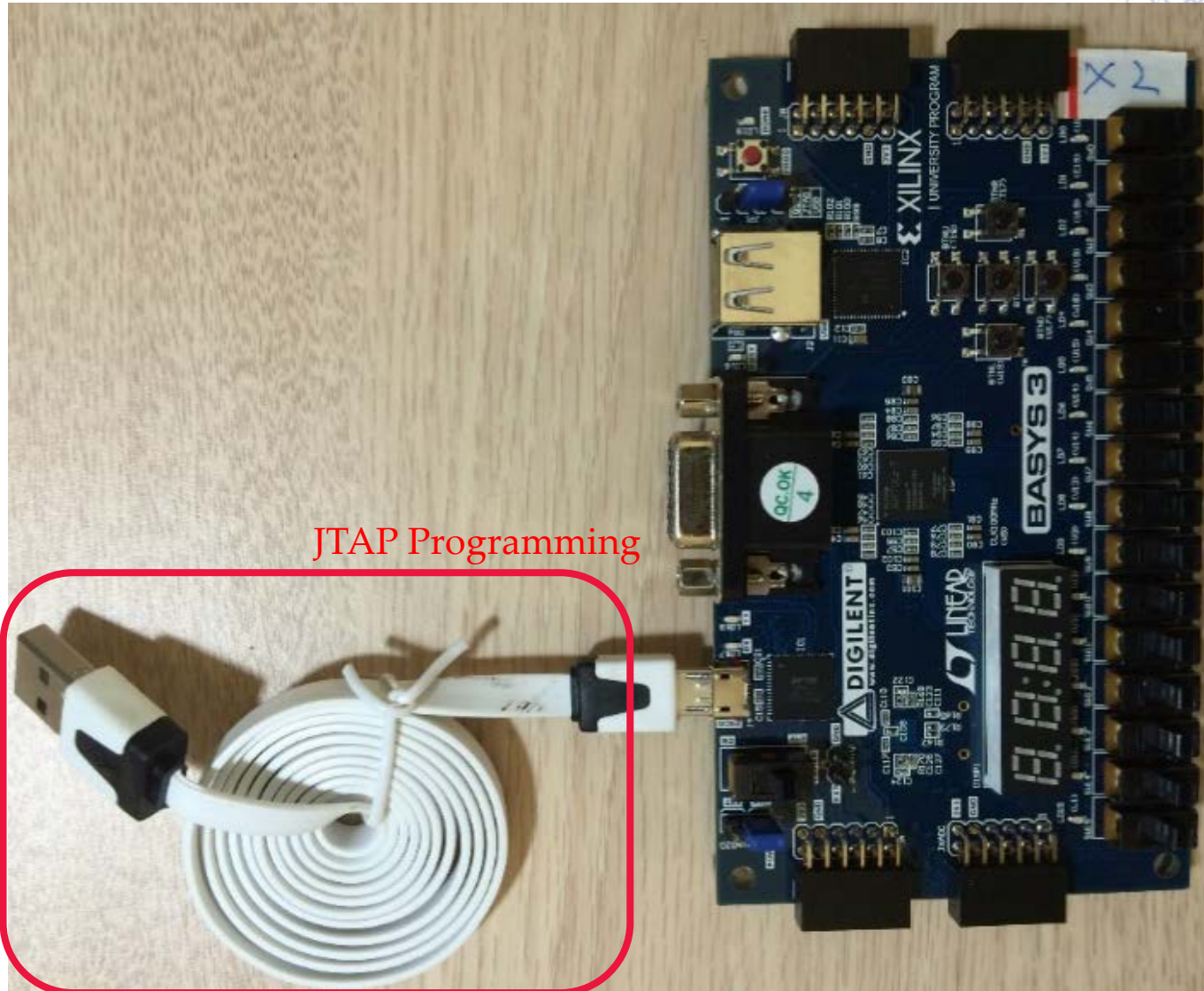
- 16 user switches
- 4-digit 7-segment display
- 12-bit VGA output
- Digilent USB-JTAG port for FPGA programming and communication

- 16 user LEDs
- Three Pmod connectors
- USB-UART Bridge
- USB HID Host for mice, keyboards and memory sticks

- 5 user pushbuttons
- Pmod for XADC signals
- Serial Flash

The complete FPGA board document (Basys3_rm.pdf) is on the course website.

JTAG Programming



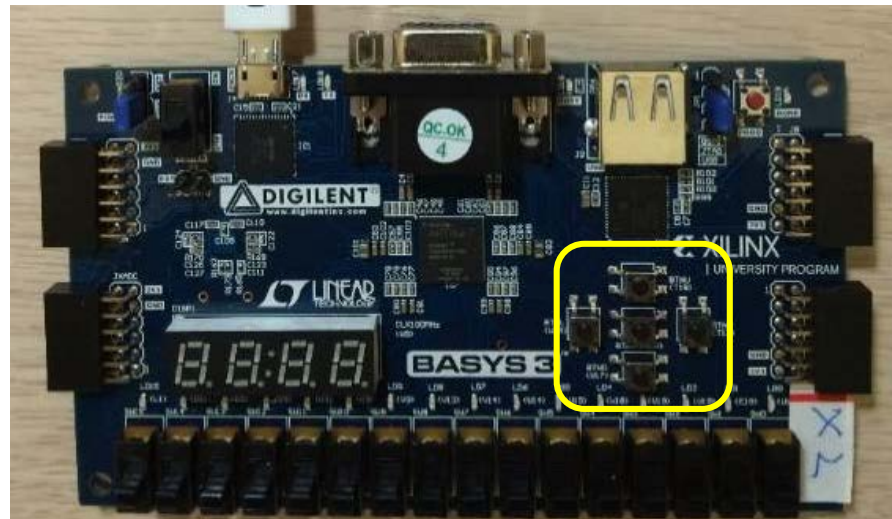
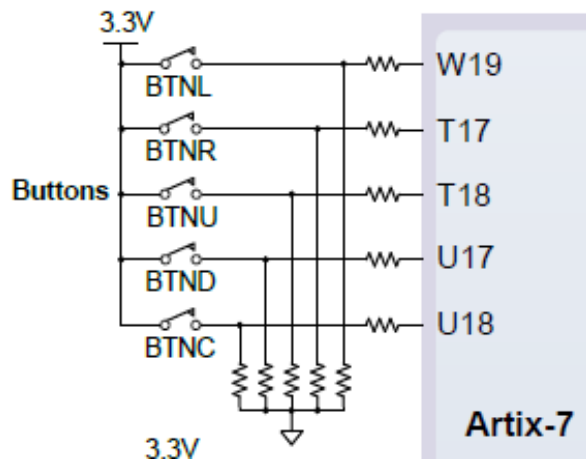
JTAG Programming

USB to PC

Specific I/Os – Push Buttons



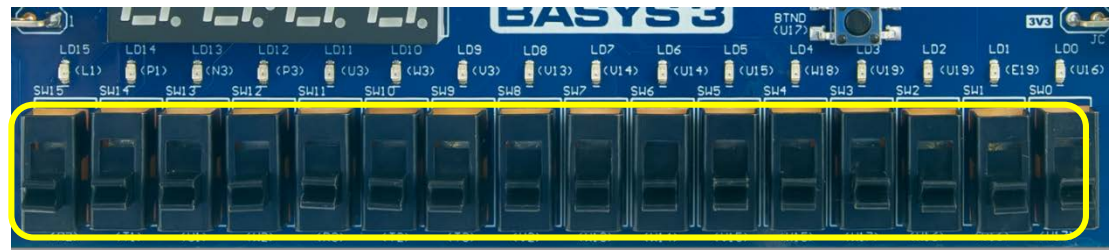
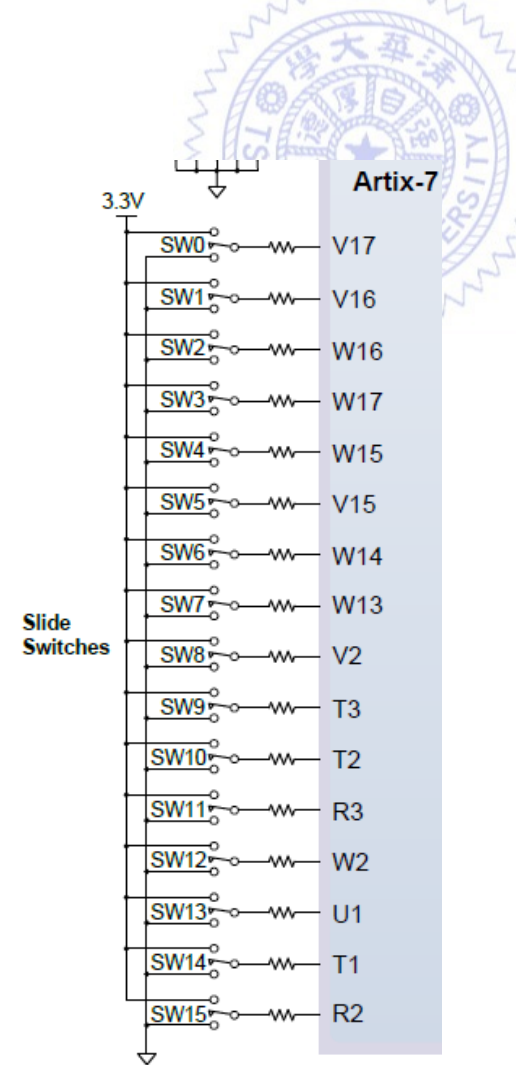
```
set_property PACKAGE_PIN W19 [get_ports {BTNL}]
set_property IOSTANDARD LVCMOS33 [get_ports {BTNL}]
set_property PACKAGE_PIN T17 [get_ports {BTNR}]
set_property IOSTANDARD LVCMOS33 [get_ports {BTNR}]
set_property PACKAGE_PIN T18 [get_ports {BTNU}]
set_property IOSTANDARD LVCMOS33 [get_ports {BTNU}]
set_property PACKAGE_PIN U17 [get_ports {BTND}]
set_property IOSTANDARD LVCMOS33 [get_ports {BTND}]
set_property PACKAGE_PIN U18 [get_ports {BTNC}]
set_property IOSTANDARD LVCMOS33 [get_ports {BTNC}]
```



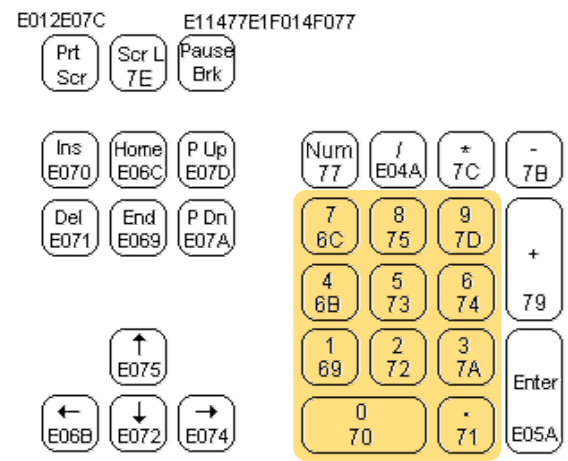
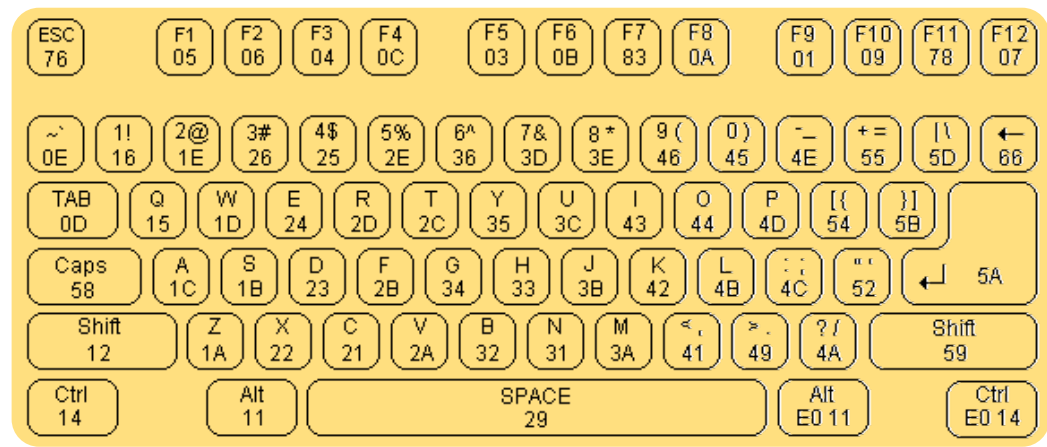
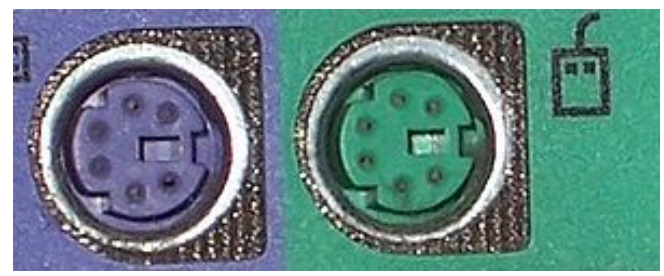
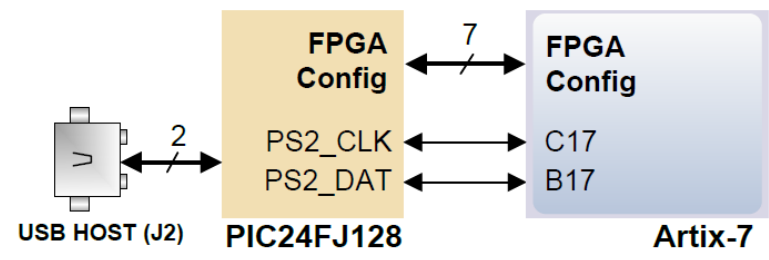
Specific I/Os – DIP Switches

```

set_property PACKAGE_PIN V17 [get_ports {SW0}]
set_property IOSTANDARD LVCMOS33 [get_ports {SW0}]
set_property PACKAGE_PIN V16 [get_ports {SW1}]
set_property IOSTANDARD LVCMOS33 [get_ports {SW1}]
set_property PACKAGE_PIN W16 [get_ports {SW2}]
set_property IOSTANDARD LVCMOS33 [get_ports {SW2}]
set_property PACKAGE_PIN W17 [get_ports {SW3}]
set_property IOSTANDARD LVCMOS33 [get_ports {SW3}]
set_property PACKAGE_PIN W15 [get_ports {SW4}]
set_property IOSTANDARD LVCMOS33 [get_ports {SW4}]
    ⋮
set_property PACKAGE_PIN T1 [get_ports {SW14}]
set_property IOSTANDARD LVCMOS33 [get_ports {SW14}]
set_property PACKAGE_PIN R2 [get_ports {SW15}]
set_property IOSTANDARD LVCMOS33 [get_ports {SW15}]
    
```



Keyboard



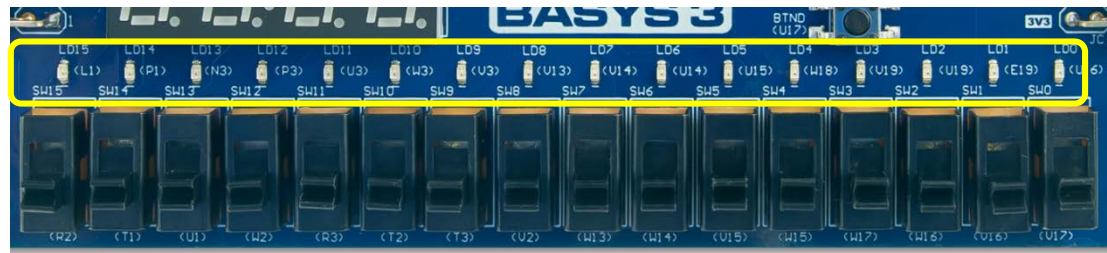
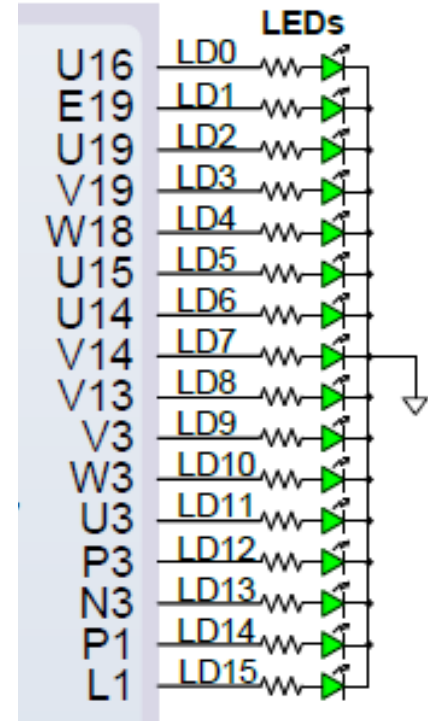


Specific I/Os - LED

```

set_property PACKAGE_PIN U16 [get_ports {LD0}]
set_property IOSTANDARD LVCMOS33 [get_ports {LD0}]
set_property PACKAGE_PIN E19 [get_ports {LD1}]
set_property IOSTANDARD LVCMOS33 [get_ports {LD1}]
set_property PACKAGE_PIN U19 [get_ports {LD2}]
set_property IOSTANDARD LVCMOS33 [get_ports {LD2}]
set_property PACKAGE_PIN W18 [get_ports {LD3}]
set_property IOSTANDARD LVCMOS33 [get_ports {LD3}]
set_property PACKAGE_PIN U15 [get_ports {LD4}]
set_property IOSTANDARD LVCMOS33 [get_ports {LD4}]
    ⋮
set_property PACKAGE_PIN P1 [get_ports {LD14}]
set_property IOSTANDARD LVCMOS33 [get_ports {LD14}]
set_property PACKAGE_PIN L1 [get_ports {LD15}]
set_property IOSTANDARD LVCMOS33 [get_ports {LD15}]

```



Specific I/Os – Segment Displays



```

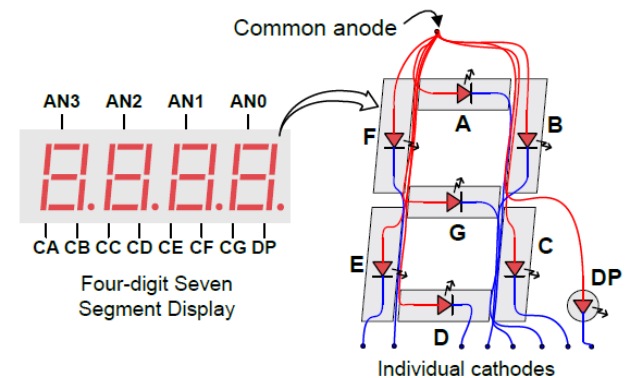
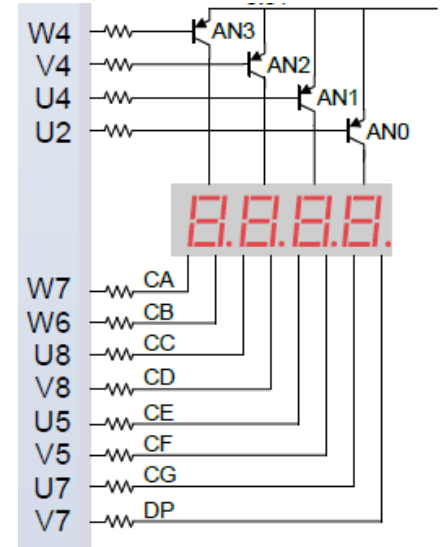
set_property PACKAGE_PIN W4 [get_ports {AN3}]
set_property IOSTANDARD LVCMOS33 [get_ports {AN3}]
set_property PACKAGE_PIN V4 [get_ports {AN2}]
set_property IOSTANDARD LVCMOS33 [get_ports {AN2}]
set_property PACKAGE_PIN U4 [get_ports {AN1}]
set_property IOSTANDARD LVCMOS33 [get_ports {AN1}]
set_property PACKAGE_PIN U2 [get_ports {AN0}]
set_property IOSTANDARD LVCMOS33 [get_ports {AN0}]
set_property PACKAGE_PIN W7 [get_ports {CA}]
set_property IOSTANDARD LVCMOS33 [get_ports {CA}]
    ⋮

```

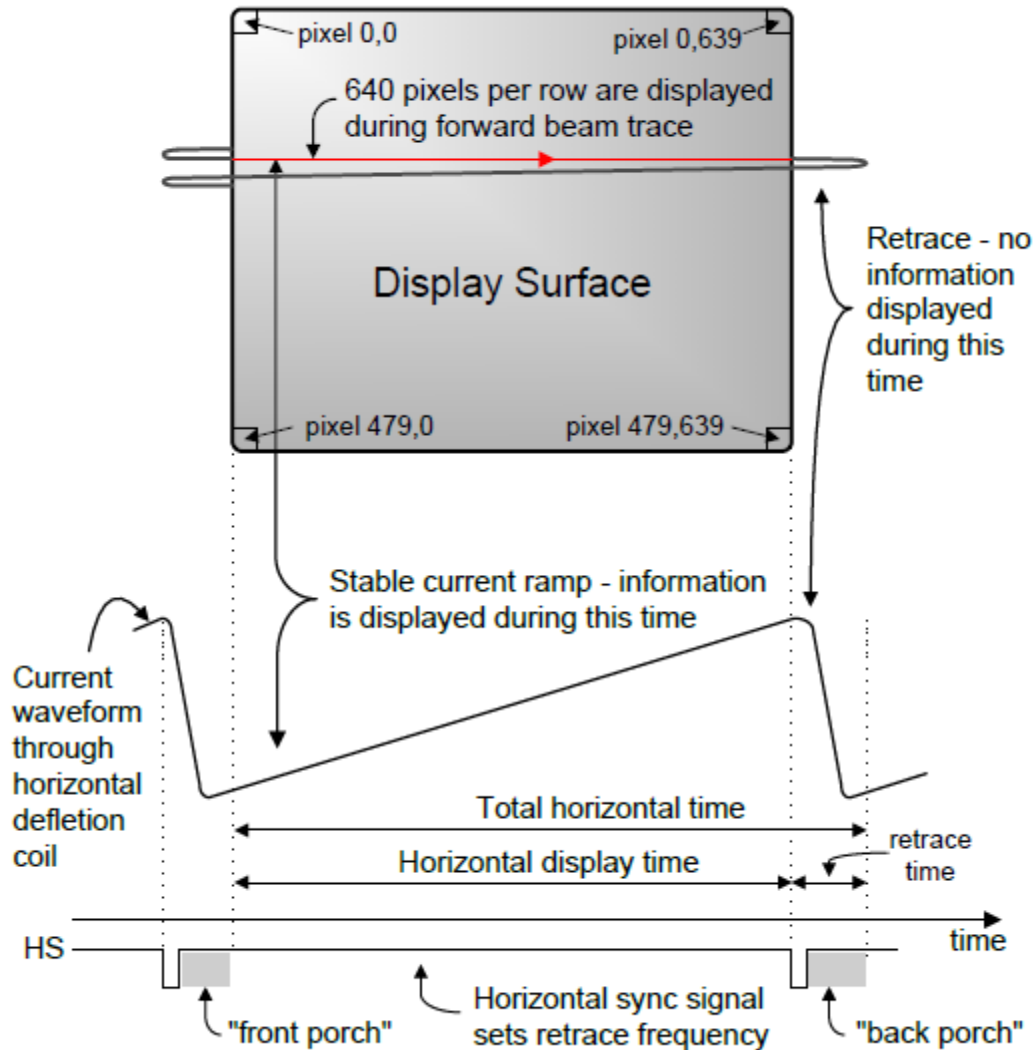
```

set_property PACKAGE_PIN V7 [get_ports {DP}]
set_property IOSTANDARD LVCMOS33 [get_ports {DP}]

```



Specific I/Os – VGA Control



Specific I/Os – VGA Control



```

set_property PACKAGE_PIN G19 [get_ports {RED0}]
set_property IOSTANDARD LVCMOS33 [get_ports {RED0}]
set_property PACKAGE_PIN H19 [get_ports {RED1}]
set_property IOSTANDARD LVCMOS33 [get_ports {RED1}]
set_property PACKAGE_PIN J19 [get_ports {RED2}]
set_property IOSTANDARD LVCMOS33 [get_ports {RED2}]
set_property PACKAGE_PIN N19 [get_ports {RED3}]
set_property IOSTANDARD LVCMOS33 [get_ports {RED3}]

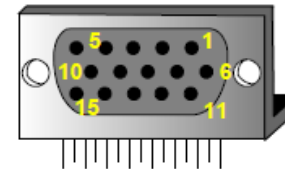
```

|
 GRN
 |
 BLU

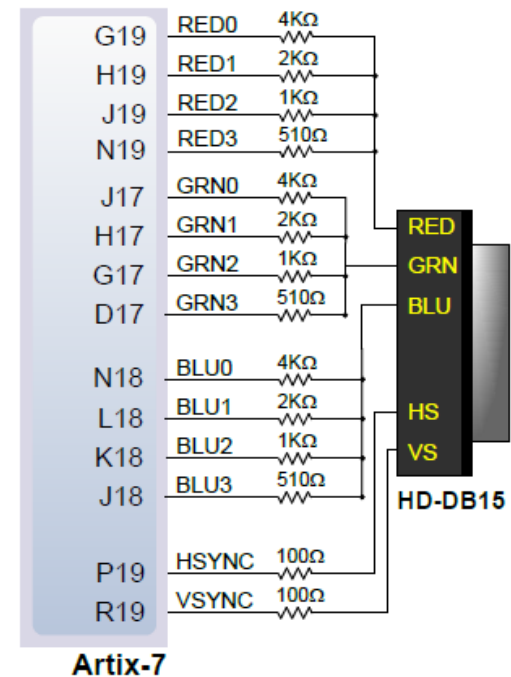
```

set_property PACKAGE_PIN P19 [get_ports {HSYNC}]
set_property IOSTANDARD LVCMOS33 [get_ports {HSYNC}]
set_property PACKAGE_PIN R19 [get_ports {VSYNC}]
set_property IOSTANDARD LVCMOS33 [get_ports {VSYNC}]

```



- Pin 1: Red
- Pin 2: Grn
- Pin 3: Blue
- Pin 13: HS
- Pin 14: VS
- Pin 5: GND
- Pin 6: Red GND
- Pin 7: Grn GND
- Pin 8: Blu GND
- Pin 10: Sync GND



Audio



```

set_property PACKAGE_PIN J1 [get_ports {JA[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {JA[0]}]
set_property PACKAGE_PIN L2 [get_ports {JA[1]}]
Set_property IOSTANDARD LVCMOS33 [get_ports {JA[1]}]
set_property PACKAGE_PIN J2 [get_ports {JA[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {JA[2]}]
set_property PACKAGE_PIN G2 [get_ports {JA[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {JA[3]}]
set_property PACKAGE_PIN H1 [get_ports {JA[4]}]
set_property IOSTANDARD LVCMOS33 [get_ports {JA[4]}]
set_property PACKAGE_PIN K2[get_ports {JA[5]}]
set_property IOSTANDARD LVCMOS33 [get_ports {JA[5]}]
set_property PACKAGE_PIN H2 [get_ports {JA[6]}]
set_property IOSTANDARD LVCMOS33 [get_ports {JA[6]}]
set_property PACKAGE_PIN G3 [get_ports {JA[7]}]
set_property IOSTANDARD LVCMOS33 [get_ports {JA[7]}]
    
```

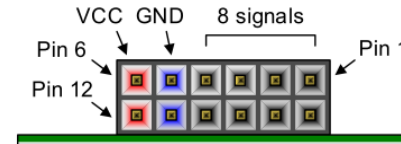


Figure 20. Pmod connectors; front view as loaded on PCB.



Pmod JA	Pmod JB	Pmod JC
JA1: J1	JB1: A14	JC1: K17
JA2: L2	JB2: A16	JC2: M18
JA3: J2	JB3: B15	JC3: N17
JA4: G2	JB4: B16	JC4: P18
JA7: H1	JB7: A15	JC7: L17
JA8: K2	JB8: A17	JC8: M19
JA9: H2	JB9: C15	JC9: P17
JA10: G3	JB10: C16	JC10: R18

Table 6. Basys3 Pmod pin assignment.

Clock



- External Clock with 100MHz frequency

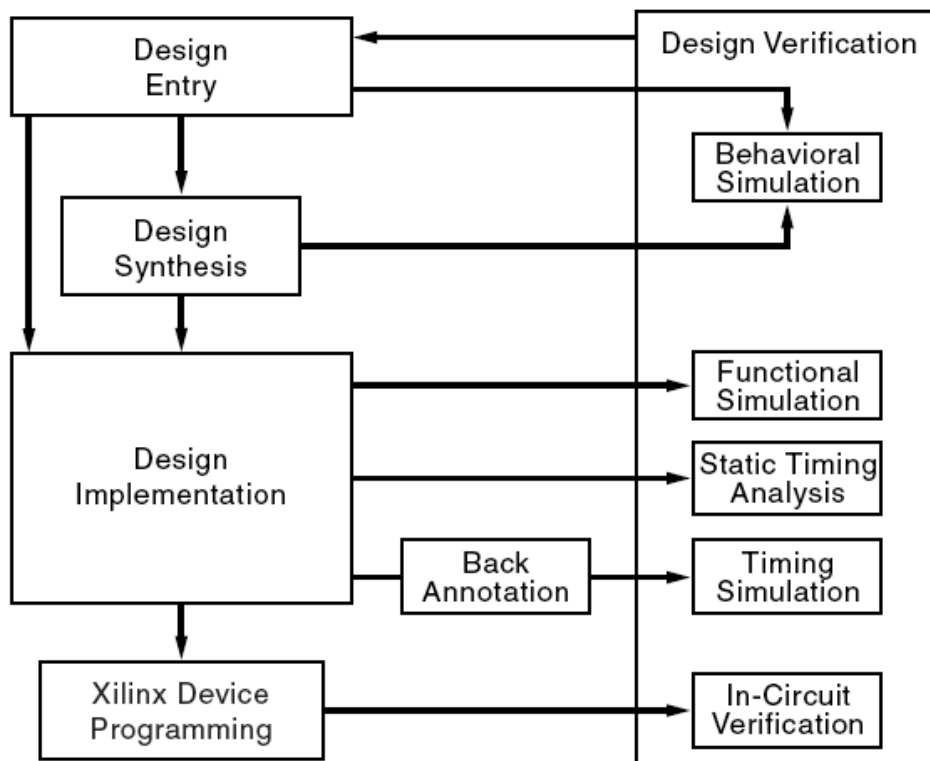
```
set_property PACKAGE_PIN W5 [get_ports {CLK}]  
set_property IOSTANDARD LVCMOS33 [get_ports {CLK}]
```



Design Flow



- General design flow
 - Design construction
 - Behavioral simulation
 - Design implementation
 - Timing simulation
- HDL-based design Flow



Important Notes



- Draw schematic first and then construct Verilog codes.
- Verilog RTL coding philosophy is not the same as C programming
 - Every Verilog RTL construct has its own logic mapping (for synthesis)
 - You should have the logics (draw schematic) first and then the RTL codes
 - You have to write **synthesizable** RTL codes

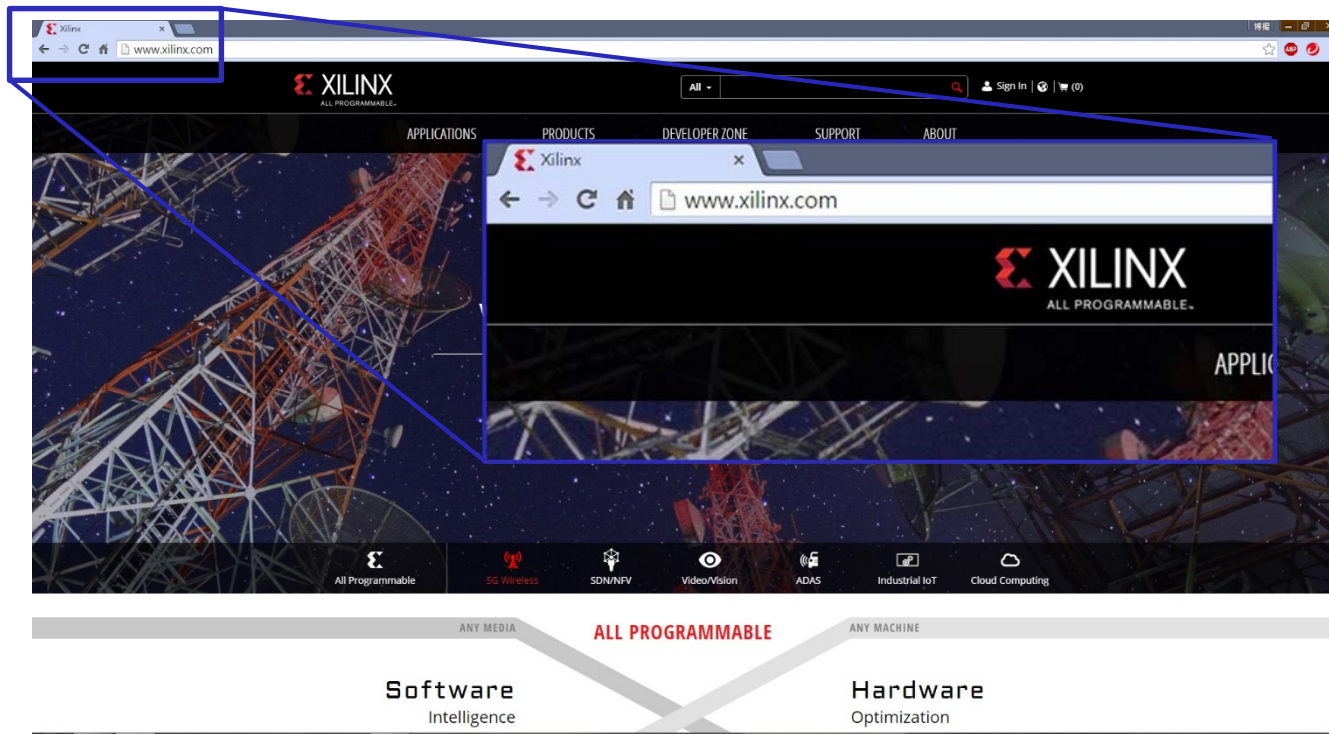


FPGA Emulation Using Xilinx Vivado

How to setup Xilinx ISE



Download link : <http://www.xilinx.com>



* You can follow the installation guide (lab0.1 Vivado Installation.pdf) in the course website.



FPGA Emulation Using Xilinx Vivado

Design Flow



- Design Source Preparation
 - Design modules (.v)
 - Design constraints (I/O pin assignments) (.xdc)
- Design Simulation
 - testbench (.v)
- Design Synthesis and Implementation

Create New Project (2/3)



Continue from previous unit slides

New Project

Default Part

Choose a default Xilinx part or board for your project. This can be changed later.

Select: **Parts** Boards

Filter

Product category: All Speed grade: -1

Family: **Artix-7** Temp grade: All Remaining

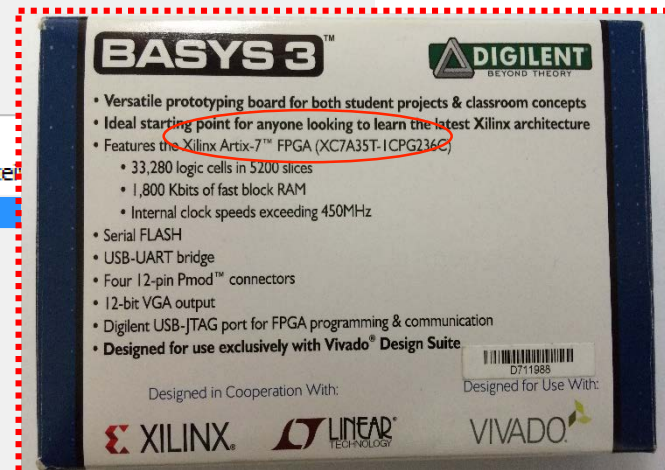
Package: **cpg236**

Reset All Filters

Search: xc7a35tcp (1 match)

Part	I/O Pin Count	Block RAMs	DSPs	FlipFlops	GTPE2 Transceivers	Gb Transceivers
xc7a35tcpg236-1	236	50	90	41600	2	2

Buttons: ? < Back Next > Finish Cancel



I/O Pins Assignment (1/4)



The screenshot shows the Vivado 2019.2 interface. In the left-hand 'Flow Navigator', the 'SYNTHESIS' section is expanded, and 'Run Synthesis' is highlighted with a red circle. A red arrow points from this button to the 'Open Synthesized Design' option in the 'Synthesis Completed' dialog box, which is also circled in red. Another red arrow points from the 'Open Synthesized Design' option to the 'OK' button, which is also circled in red. The text 'double click' is written in red below the 'Run Synthesis' button. The 'Design Runs' table at the bottom shows the status of the synthesis run.

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy
synth_1	constrs_1	synth_design Complete!								1	0	0.0	0	0	2/10/20, 3:56 PM	00:00:34	Vivado Synthesis Defaults (Vivado Synthesis 2019)
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implement

I/O Pins Assignment (2/4)



3

Remember to save your assignment

1

The screenshot shows the Vivado 2019.2 interface. The 'I/O Ports' table is visible, and the 'Save Constraints' dialog is open. Red arrows and boxes highlight key steps: saving the assignment, changing the I/O standard to LVCMOS33, and saving the constraints file.

Name	Direction	Interface	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std	Vcco	Vref	Drive Strength
a	IN			V17	<input checked="" type="checkbox"/>	14	LVCMOS33*	3.300		
b	IN			V16	<input checked="" type="checkbox"/>	14	LVCMOS33*	3.300		
out	OUT			U16	<input checked="" type="checkbox"/>	14	LVCMOS33*	3.300		12
sel	IN			W16	<input checked="" type="checkbox"/>	14	LVCMOS33*	3.300		

Save Constraints dialog details:

- File type: XDC
- File name: smux.xdc
- File location: <Local to Project>
- Radio button: Create a new file

2

change to LVCMOS33

4

I/O Pins Assignment (3/4)



The screenshot displays the Vivado I/O Planning tool interface. A 'Confirm Close' dialog box is overlaid on the 'I/O Port Properties' window, asking 'OK to close 'Synthesized Design'?'. The 'I/O Port Properties' window shows the configuration for the 'out' port, including its direction (OUT), package pin (U16), and site information (IOB_X0Y3).

The 'I/O Ports' table at the bottom of the interface provides a detailed overview of the pin assignments:

Name	Direction	Interface	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std	Vcco	Vref	Drive Strength	Slew Type	Pull Type	Off-Chip Termination	IN_TERM
a	IN			V17	<input checked="" type="checkbox"/>	14	LVCMOS33*	3.300				NONE	NONE	
b	IN			V16	<input checked="" type="checkbox"/>	14	LVCMOS33*	3.300				NONE	NONE	
out	OUT			U16	<input checked="" type="checkbox"/>	14	LVCMOS33*	3.300	12		SLOW	NONE	FP_VTT_50	
sel	IN			W16	<input checked="" type="checkbox"/>	14	LVCMOS33*	3.300				NONE	NONE	

I/O Pins Assignment (4/4)



The screenshot shows the Vivado 2019.2 interface. On the left, the 'PROJECT MANAGER' pane shows the project hierarchy with 'smux.xdc (target)' circled in red and the text 'double click' next to it. The 'Source File Properties' pane for 'smux.xdc' shows it is enabled and located at 'C:/Users/hp/LD/smux/smux.srcs/constrs_1/new'. The main editor window shows the 'smux.xdc' file with the following content:

```
1 : set_property IOSTANDARD LVCMOS33 [get_ports a]
2 : set_property IOSTANDARD LVCMOS33 [get_ports b]
3 : set_property IOSTANDARD LVCMOS33 [get_ports sel]
4 : set_property PACKAGE_PIN V17 [get_ports a]
5 : set_property PACKAGE_PIN V16 [get_ports b]
6 : set_property PACKAGE_PIN W16 [get_ports sel]
7 : set_property PACKAGE_PIN U16 [get_ports out]
8 : set_property IOSTANDARD LVCMOS33 [get_ports out]
9 :
```

At the bottom, the 'Design Runs' table shows the current synthesis status:

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy
synth_1	constrs_1	Synthesis Out-of-date								1	0	0.0	0	0	2/10/20, 3:56 PM	00:00:34	Vivado Synthesis Defaults (Vivado Synthesis 2019)
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implement)

Or you can create the file directly and then added by "Add Sources" (constraints)

Synthesis and Implementation (1/7)



Flow Navigator

PROJECT MANAGER - smux

Sources

- Design Sources (1)
 - smux (smux.v)
- Constraints (1)
 - constrs_1 (1)
- Simulation Sources (1)
 - sim_1 (1)

Hierarchy Libraries Compile Order

Constraint Set Properties

constrs_1

Default directory: C:/Users/hp/LD/smux/smux

File count: 1

Format: XDC

Target constraint file: smux.xdc

Active

General Properties

Project Summary

```
1 : set_property IOSTANDARD LVCMOS33 [get_ports a]
2 : set_property IOSTANDARD LVCMOS33 [get_ports b]
3 : set_property IOSTANDARD LVCMOS33 [get_ports sel]
4 : set_property PACKAGE_PIN V17 [get_ports a]
5 : set_property PACKAGE_PIN V16 [get_ports b]
6 : set_property PACKAGE_PIN W16 [get_ports sel]
7 : set_property PACKAGE_PIN U16 [get_ports out]
8 : set_property IOSTANDARD LVCMOS33 [get_ports out]
```

Synthesis is Out-of-date

If this window pops up, press "Yes"

Synthesis is out-of-date. OK to launch synthesis and implementation first?
'Generate' Bitstream' will automatically start when synthesis and implementation completes.

Don't show this dialog again

Yes No Cancel

Tcl Console Messages Log Reports Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy
synth_1	constrs_1	Synthesis Out-of-date								1	0	0.0	0	0	2/10/20, 3:56 PM	00:00:34	Vivado Synthesis Defaults (Vivado Synthesis 2019)
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implement

double click

Generate a programming file after implementation

Synthesis and Implementation (2/7)



implementation progress information

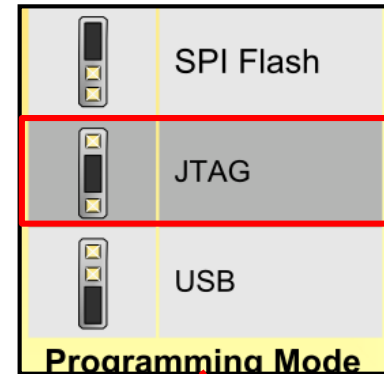
The screenshot shows the Vivado 2019.2 IDE interface. The top menu bar includes File, Edit, Flow, Tools, Reports, Window, Layout, View, and Help. A red circle highlights the 'Running synth_design' button in the top right corner, with 'Cancel' and a green checkmark icon next to it. The 'Flow Navigator' on the left shows the project hierarchy: PROJECT MANAGER (Sources, Constraints, Simulation Sources), IP INTEGRATOR, SIMULATION, RTL ANALYSIS, SYNTHESIS (Run Synthesis), IMPLEMENTATION (Run Implementation), and PROGRAM AND DEBUG. The 'Constraint Set Properties' window for 'constrs_1' shows the default directory, file count (1), format (XDC), and target constraint file (smux.xdc). The 'Design Runs' table at the bottom shows the current synthesis run status.

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy
synth_1	constrs_1	Running synth_design...													2/10/20, 4:19 PM	00:00:00	Vivado Synthesis Defaults (Vivado Synthesis 2019)
impl_1	constrs_1	Queued...														00:00:00	Vivado Implementation Defaults (Vivado Implement)

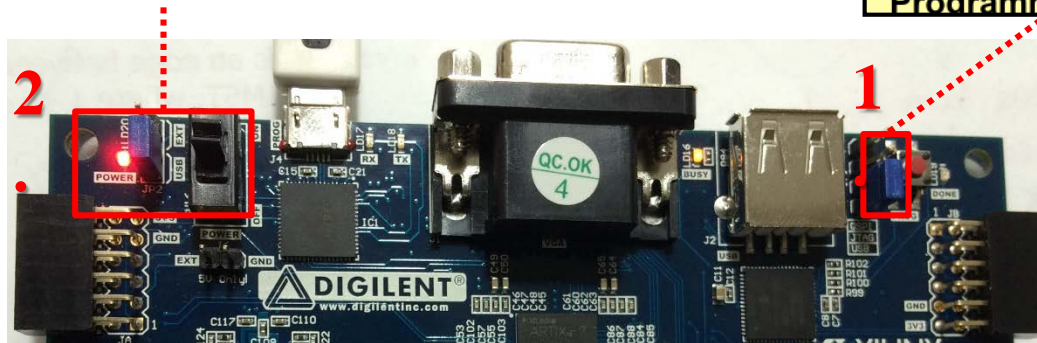


Power-on and JTAG-Mode

Step 1:
Change blue jumper to [**JTAG**] mode



Step 2:
Turn the power switch to [**ON**]



Synthesis and Implementation (3/7)



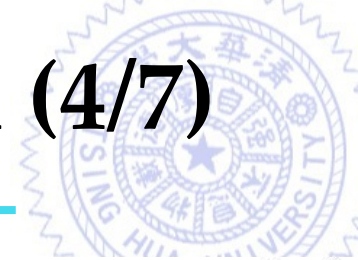
1 Connect and power on the FPGA board

The screenshot shows the Vivado 2019.2 interface. On the left, the 'Flow Navigator' pane shows the project flow: PROJECT MANAGER, SIMULATION, SYNTHESIS, and IMPLEMENTATION. The 'Run Synthesis' and 'Open Synthesized Design' steps are circled in blue. The 'Open Implemented Design' step is also circled in blue. In the center, a 'Bitstream Generation Completed' dialog box is open, with the 'Open Hardware Manager' option selected and circled in red. A blue box with the number '2' is placed over the dialog. The background shows the 'Sources' pane with 'smux' and 'constrs_1' selected, and the 'Design Runs' table at the bottom.

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy
synth_1	constrs_1	synth_design Complete!								1	0	0.0	0	0	2/10/20, 4:19 PM	00:00:44	Vivado Synthesis Defaults (Vivado Synthesis 2
impl_1	constrs_1	write_bitstream Complete!	NA	NA	NA	NA	NA	1.103	0	1	0	0.0	0	0	2/10/20, 4:20 PM	00:01:09	Vivado Implementation Defaults (Vivado Impl

After synthesis and implementation

Synthesis and Implementation (4/7)



The screenshot shows the Vivado 2019.2 IDE interface. The top menu bar includes File, Edit, Flow, Tools, Reports, Window, Layout, View, and Help. The main workspace is divided into several panes:

- Flow Navigator:** Shows the project flow with sections for PROJECT MANAGER, IP INTEGRATOR, SIMULATION, RTL ANALYSIS, SYNTHESIS, IMPLEMENTATION, and PROGRAM AND DEBUG. The 'Open Hardware Manager' option is selected under the PROGRAM AND DEBUG section.
- HARDWARE MANAGER - unconnected:** Displays a message: "No hardware target is open. Open target". A context menu is open over this message, with "Auto Connect" highlighted. Other options include "Recent Targets", "Available Targets on Server", and "Open New Target...".
- Constraint Set Properties:** Shows properties for "constrs_1", including the default directory (C:/Users/hp/LD/smux/smux.srcs/c), file count (1), format (XDC), and target constraint file (smux.xdc).
- Code Editor:** Displays the content of "smux.xdc" with the following text:

```
1 timescale 1ns / 1ps
2 //-----
3 //Company:
4 //Engineer:
5 //
6 //Create Date: 02/10/2020 01:16:53 PM
7 //Design Name:
8 //Module Name: smux
9 //Project Name:
10 //Target Devices:
11 //Tool Versions:
12 //Description:
13 //
14 //Dependencies:
15 //
16 //Revision:
17 //Revision 0.01 - File Created
18 //Additional Comments:
19 //
20 //-----
21
```
- Tcl Console:** Shows the execution of the command "launch_runs impl_1 -to_step write_bitstream". The output indicates that the synthesis and implementation processes were launched successfully, with run output captured in log files.

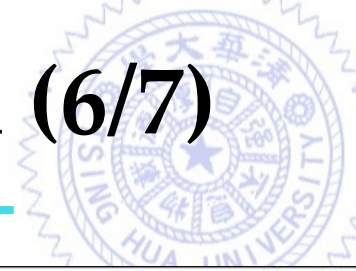
Synthesis and Implementation (5/7)



The screenshot displays the Vivado 2019.2 interface during the implementation phase. The Hardware Manager window shows the selected device 'xc7a35t_0' with a 'Program...' button circled in red. The Hardware Device Properties window shows the device name 'xc7a35t_0' and part 'xc7a35t'. The Program Device dialog box is open, showing the bitstream file path 'impl_1/smux.bit' selected. The Tcl Console shows the command 'program_hw_device' and its output.

```
INFO: [Labtools1stcl 44-466] Opening hw_target localhost:3121/xilinx_tcf/Digilent/210183AA1033A
open_hw_target: Time (s): cpu = 00:00:04 ; elapsed = 00:00:09 . Memory (MB): peak = 3010.063 ; gain = 1078.758
set_property PROGRAM_FILE [C:/Users/hp/LD/smux/smux.srscs/sources_1/new/smux.v] [get_hw_devices xc7a35t_0]
current_hw_device [get_hw_devices xc7a35t_0]
refresh_hw_device -update_hw_probes false [index [get_hw_devices xc7a35t_0] 0]
INFO: [Labtools 27-1434] Device xc7a35t (JTAG device index = 0) is programmed with a design that has no supported debug core(s) in it.
```

Synthesis and Implementation (6/7)

The screenshot displays the Vivado 2019.2 software interface. The top menu bar includes File, Edit, Flow, Tools, Reports, Window, Layout, View, and Help. The main workspace is divided into several panes:

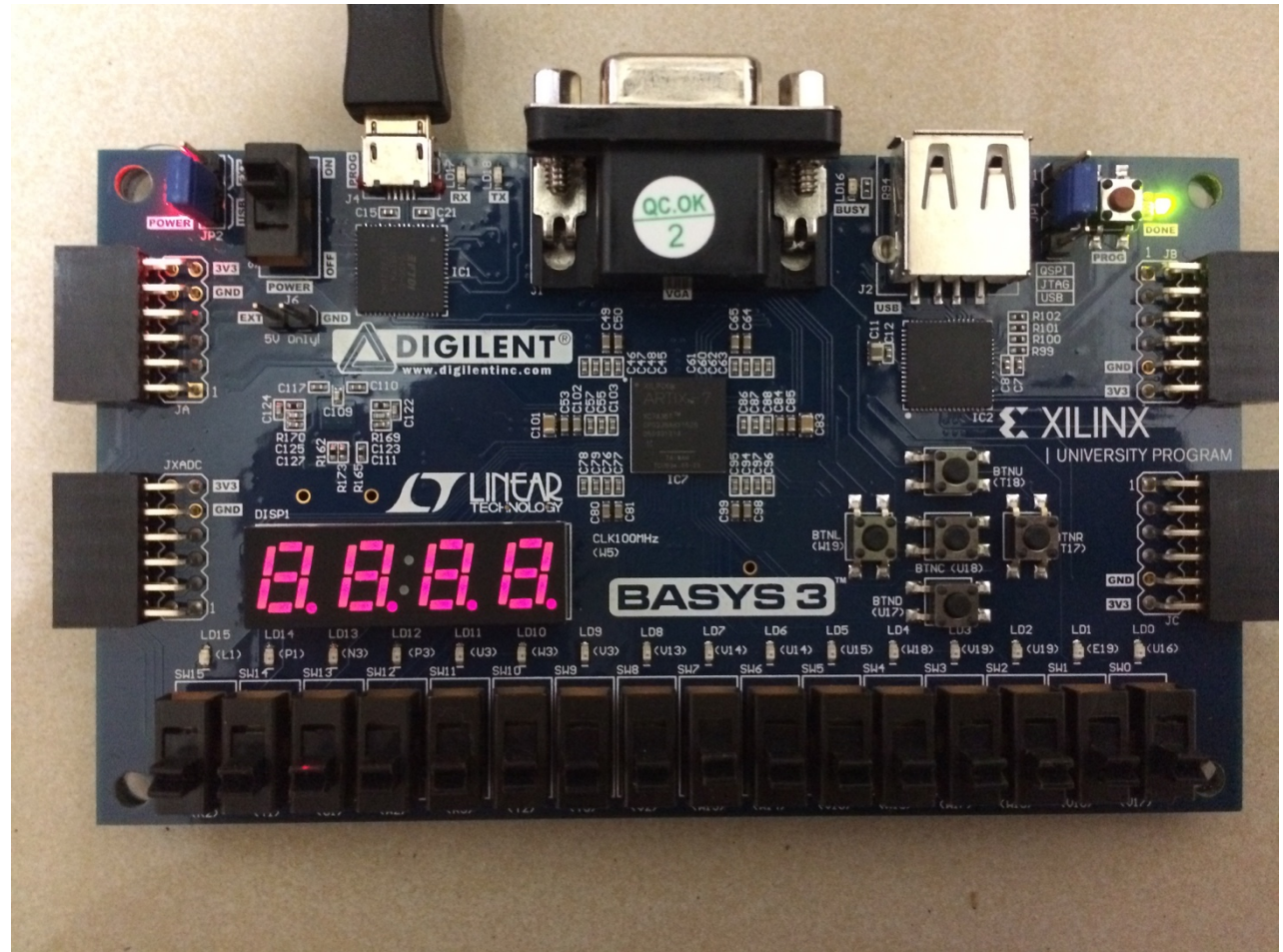
- Flow Navigator:** Shows the project's progress through various stages, with 'PROGRAM AND DEBUG' selected.
- PROJECT MANAGER:** Lists project settings, IP Catalog, and IP Integrator options.
- HARDWARE MANAGER:** Displays the hardware configuration for 'localhost/xilinx_tcf/Digilent/210183AA1033A'. It shows a table of hardware components, including 'xc7a35t_0 (1)' which is in a 'Program...' state. Below this, the 'Hardware Device Properties' for 'xc7a35t_0' are shown, including Name, Part, ID code, IR length, and Status (Programmed).
- Code Editor:** Shows the 'smux.v' source file with a Verilog-like code snippet starting with a timescale and various comments.
- Tcl Console:** Shows the execution of Tcl commands for programming the device, such as 'set_property FULL_PROBES.FILE 1 [get_hw_devices xc7a35t_0]' and 'program_hw_devices [get_hw_devices xc7a35t_0]'. The console output indicates that the device 'xc7a35t_0' is programmed with a design that has no supported debug core(s) in it.

In the top right corner of the Vivado window, a status bar shows 'write_bitstream Complete' with a green checkmark, which is circled in red.

Result



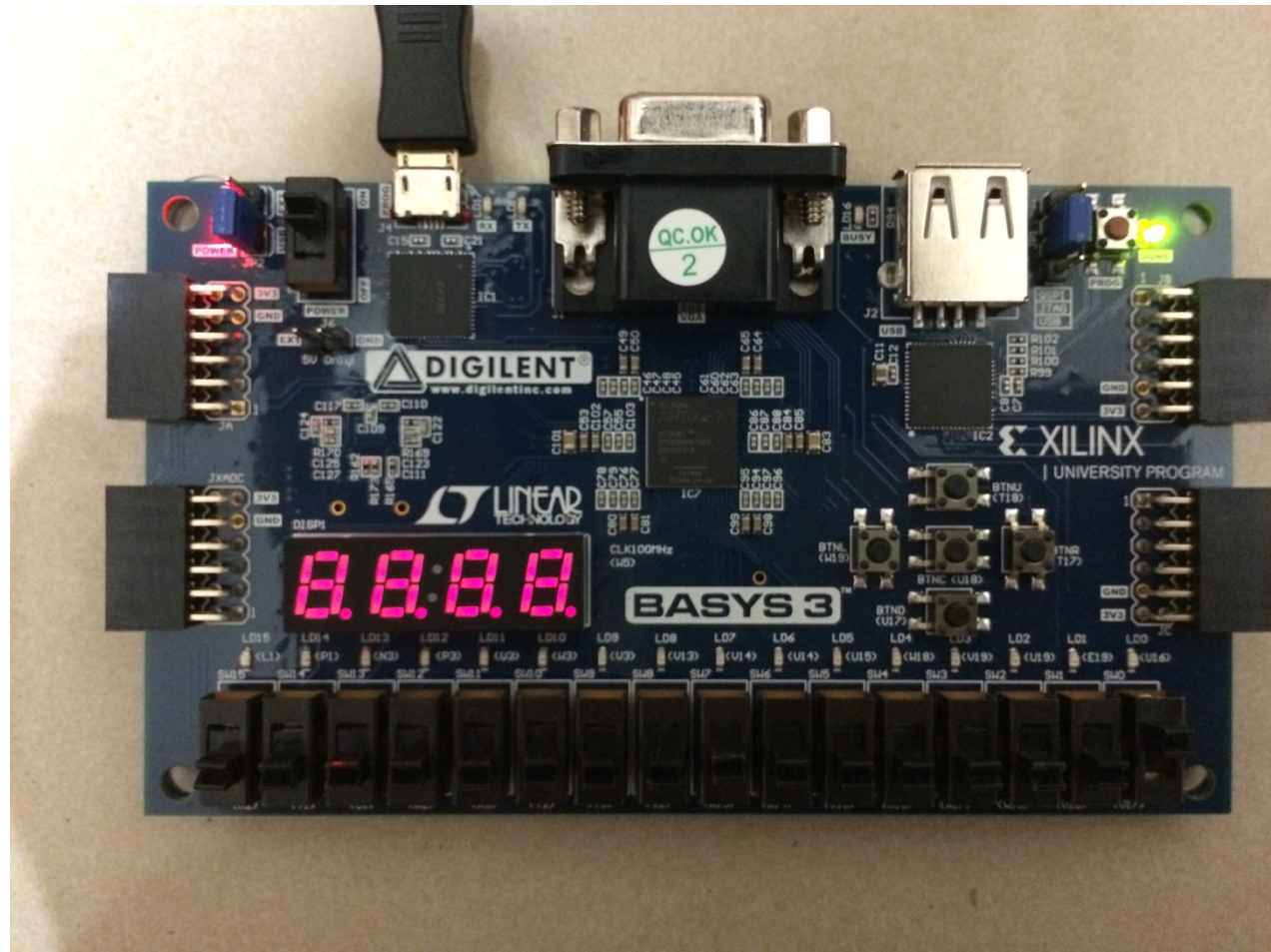
sel = 0
a = 0
b = 0



Result



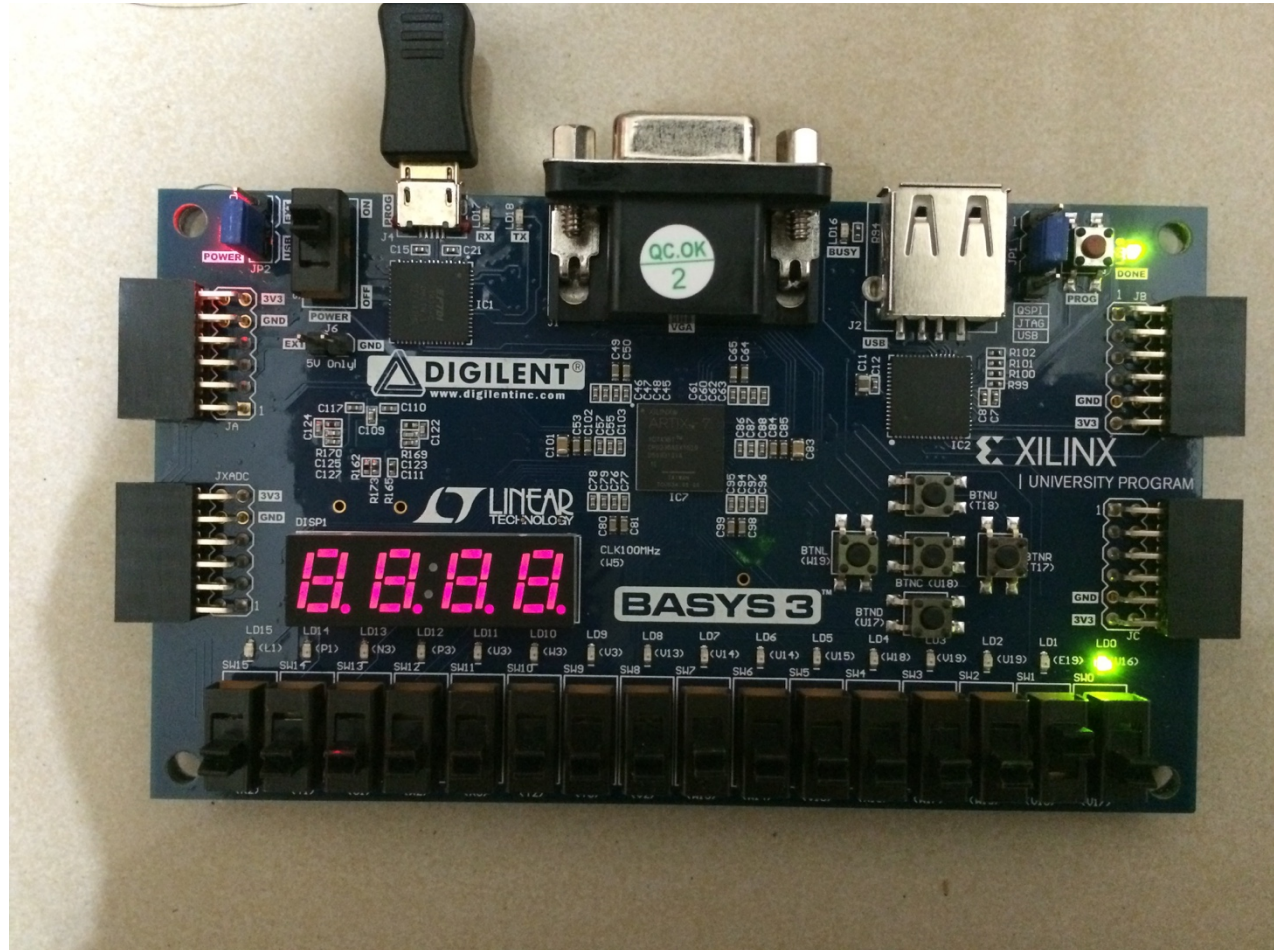
sel = 0
a = 1
b = 0



Result



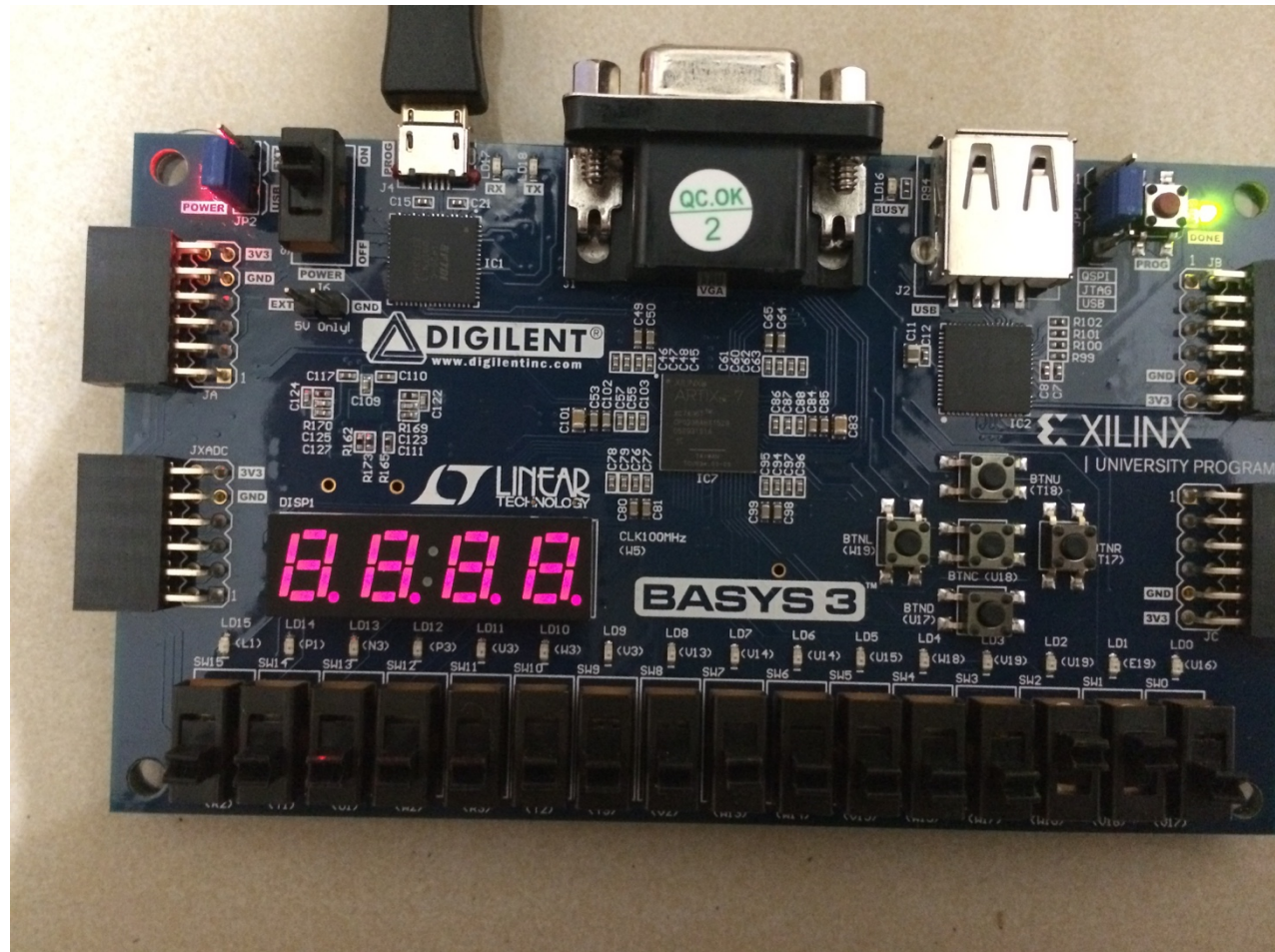
sel = 0
a = 0
b = 1



Result



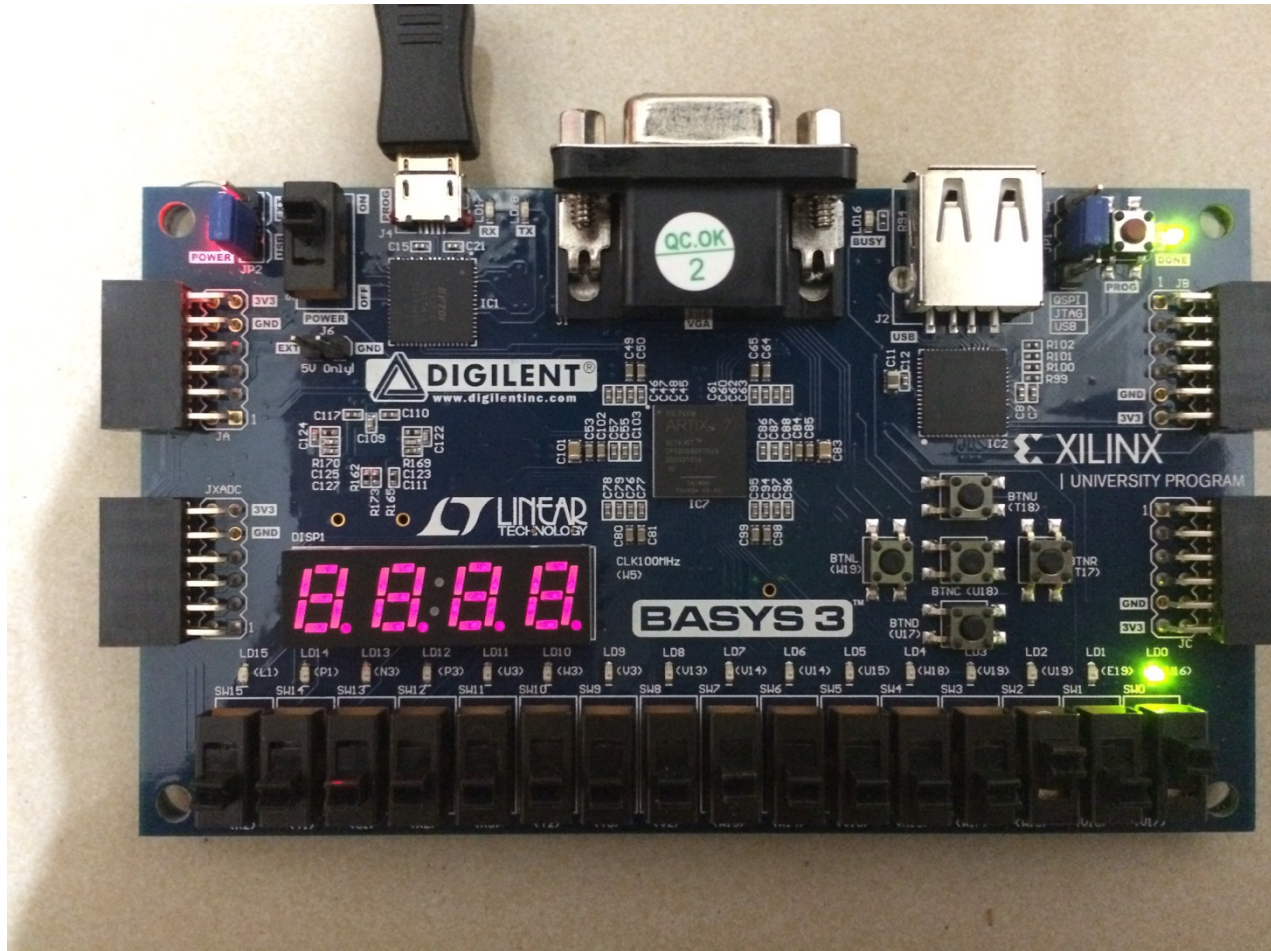
sel = 1
a = 0
b = 1



Result



sel = 1
a = 1
b = 0





Verilog RTL Code Examples



```
`timescale 1ns / 1ps

module SMUX(
    out, // multiplexer output
    a, // multiplexer input a
    b, // multiplexer input b
    sel // selection control signal
);
output out; // multiplexer output
input a,b; // two inputs to be selected
input sel; // selection control signal

// multiplexer function
assign out = (sel) ? a : b ;

endmodule
```

```
`timescale 1ns / 1ps

module SMUX(
    out, // multiplexer output
    a, // multiplexer input a
    b, // multiplexer input b
    sel // selection control signal
);
output out; // multiplexer output
input a,b; // two inputs to be selected
input sel; // selection control signal

reg out; // multiplexer output

// multiplexer function
always @(a or b or sel)
    out = (sel) ? a : b ;

endmodule
```