



EECS 207002

Logic Design Laboratory

邏輯設計實驗

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Syllabus



- Credit : 3
- Instructor : Yuan-Hao Huang (黃元豪)
 - Room 953 Delta Building,
 - E-mail : yhhuang@ee.nthu.edu.tw
- Class Hours
 - 15:30~17:20 (T7,T8) Teaching at Delta Building Room 216 (class)
- TA Hours
 - 17:30~19:20 (T9,TA) Delta Building 2F 電子電路實驗室(lab)
 - 17:30~19:20 (M9,MA) Delta Building 2F 電子電路實驗室(lab)
補demo 於 Prof. His-Pin Ma's TA Hours
- Course Notes : iLMS
- Teaching Assistants:
 - 島津達則 <king3789914@yahoo.com.tw>

Syllabus



- Reference Book

- William J. Dally & R. Curtis Harting, *Digital Design – A System Approach*, Cambridge International Student Edition
- M. Morris Mano & Charles R. Kime, *Logic and Computer Design Fundamental*, 4th ed. 2008, Pearson Prentice Hall.

- Grading

- 70% : Experiments
- 20% : Final Project
- 10% : Final On-Site Examination

Schedule



Official Week	Date	Content
1	3/3	Introduction to Verilog RTL (lab 0)
2	3/10	FPGA Emulation (lab 1)
3	3/17	Counters and Shift Registers I (lab 2)
4	3/24	Counters and Shift Registers II (lab 3)
5	3/31	Timers (lab 4)
6	4/7	Electronic Clock I (Time Display) (lab 5)
7	4/14	Electronic Clock II (Multi-Function) (lab 6)
8	4/21	Speaker (lab 7)
9	4/28	Keyboard (lab 8)
10	5/5	Keyboard (lab 9)
11	5/12	Electronic Organ (lab 9) final project proposal
12	5/19	Final Exam (lab 10)
13	5/26	Final Project
14	6/2	Final Project
15	6/9	Final Project
16	6/16	Final Project
17	6/19	Final Project deadline

Experiments



- Pre-lab assignment
 - Upload simulation results and signed by TAs
- Course contents
 - ~40min instruction by instructor
- Lab Experiments
 - Rest of the lab hours with instructor & TAs
 - Demo by pm 17:20
- Lab Demo Report deadline
 - 1 day after demo (pm 11:59, Wednesday)
 - 1 day after Monday's 補demo (pm 11:59, Tuesday)

Lab Evaluation



- Pre-lab
 - On time: 20% (-5%/week)
- Experiment
 - On time: 35% (-5%/week)
- Lab report
 - On time: 15% (-5%/week)
 - Report score: +20%
 - Bonus Problem: +10%

Software



- Vivado Installation
 - Verilog HDL Editor
 - Verilog Simulator
 - FPGA Design and Implementation Tool
- You can download the tool package at
 - <http://www.Xilinx.com>



電子電路設計學程

建議修課時程

大一

入門課程

邏輯設計
EE 2280

邏輯設計實驗
EE 2230

計算機程式語言
EE 2310

大二

核心課程

電子學
EE 2250

電路學
EE 2210

積體電路設計導論
EE 4290

數位電路分析與設計
EE 3680

訊號與系統
EE 3610

電子電路實驗
EE 2270

資料結構
EE 2410

大三

實作專題
EE 3900

類比電路分析與設計
EE 3680

計算機結構
EE 3450

積體電路設計實習
EE 4292

嵌入式系統與實驗
EE2405

大四
研究所

核心課程

*超大型積體電路設計
EE5250

超大型積體電路測試
EE6250

積體電路設計自動化
EE5265

*若無修過EE4290則需修EE5250

進階課程

射頻積體電路設計
EE5280

有線通訊積體電路設計
EE5285

混合式無線通訊積體電路設計
EE5665

超大型積體電路數位訊號處理
EE5270

計算機算數
EE5410

仿神經積體電路設計
EE6260

半導體記憶體測試
EE6253

通訊系統晶片設計
COM5190

類比電路設計
ENE5210