EECS 207002
Logic Design Laboratory
邏輯設計實驗

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Syllabus

- Credit : 3
- Instructor : Yuan-Hao Huang (黃元豪)
  - Room 953 Delta Building,
  - E-mail : yhhuang@ee.nthu.edu.tw
- Class Hours
  - 15:30~17:20 (T7,T8) Teaching at Delta Building Room 216 (class)
- TA Hours
  - 17:30~19:20 (T9,TA) Delta Building 2F 電子電路實驗室(lab)
  - 17:30~19:20 (M9,MA) Delta Building 2F 電子電路實驗室(lab)
    補demo 於 Prof. His-Pin Ma's TA Hours
- Course Notes : iLMS
- Teaching Assistants:
  - 島津達則 <king3789914@yahoo.com.tw>

Syllabus

- Reference Book
  - William J. Dally & R. Curtis Harting, *Digital Design – A System Approach*, Cambridge International Student Edition
  - M. Morris Mano & Charles R. Kime, Logic and Computer Design Fundamental, 4th ed. 2008, Pearson Prentice Hall.

- Grading
  - 70% : Experiments
  - 20% : Final Project
  - 10% : Final On-Site Examination

Schedule

Official Week	Date	Content
1	3/3	Introduction to Verilog RTL (lab 0)
2	3/10	FPGA Emulation (lab 1)
3	3/17	Counters and Shift Registers I (lab 2)
4	3/24	Counters and Shift Registers II (lab 3)
5	3/31	Timers (lab 4)
6	4/7	Electronic Clock I (Time Display) (lab 5)
7	4/14	Electronic Clock II (Multi-Function) (lab 6)
8	4/21	Speaker (lab 7)
9	4/28	Keyboard (lab 8)
10	5/5	Keyboard (lab 9)
11	5/12	Electronic Organ (lab 9) final project proposal
12	5/19	Final Exam (lab 10)
13	5/26	Final Project
14	6/2	Final Project
15	6/9	Final Project
16	6/16	Final Project
17	6/19	Final Project deadline

Experiments

- Pre-lab assignment
  - Upload simulation results and signed by TAs
- Course contents
  - ~40min instruction by instructor
- Lab Experiments
  - Rest of the lab hours with instructor & TAs
  - Demo by pm 17:20
- Lab Demo Report deadline
  - 1 day after demo (pm 11:59, Wednesday)
  - 1 day after Monday's 補demo (pm 11:59, Tueday)

Lab Evaluation

- Pre-lab
  - On time: 20% (-5%/week)
- Experiment
  - On time: 35% (-5%/week)
- Lab report
  - On time: 15% (-5%/week)
  - Report score: +20%
  - Bonus Problem: +10%

Software

- Vivado Installation
  - Verilog HDL Editor
  - Verilog Simulator
  - FPGA Design and Implementation Tool
- You can download the tool package at
    - http://www.Xilinx.com

電子電路設計學程

建議修課時程