I²S

I²S (**Inter-IC Sound**), pronounced eye-squared-ess, is an electrical serial bus interface standard used for connecting digital audio devices together. It is used to communicate PCM audio data between integrated circuits in an electronic device. The I²S bus separates clock and serial data signals, resulting in simpler receivers than those required for asynchronous communications systems that need to recover the clock from the data stream. Alternatively I²S is spelled **I2S** (pronounced eye-two-ess) or **IIS** (pronounced eye-eye-ess). Despite the similar name, I²S is unrelated to the bidirectional I²C (IIC) bus.

I²S

Type	Bus
Production history	
Designer	Philips Semiconductor, known today as NXP Semiconductors
Designed	1986
Data	
Data signal	Push-Pull
Width	1 data line (SD) + 2 clock lines (SCK, WS)
Protocol	Serial

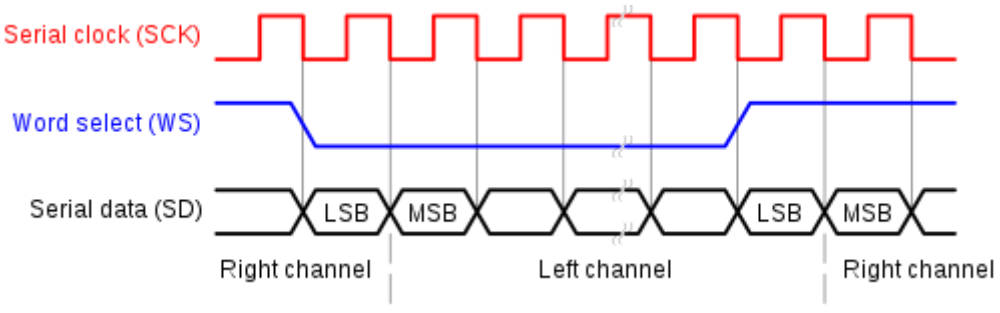
Contents

History

This standard was introduced in 1986 by Philips Semiconductor (now NXP Semiconductors) and was last revised on June 5, 1996.[1]

Details

The I²S protocol outlines one specific type of PCM digital audio communication with defined parameters outlined in the Philips specification.



Timing diagram of I²S

The bus consists of at least three lines:

1. Bit clock line
   - Officially "continuous serial clock (SCK)".[1] Typically written "bit clock (BCLK)".[2]
2. Word clock line

- Officially "word select (WS)".[1] Typically called "left-right clock (LRCLK)"[2] or "frame sync (FS)".[3]
- 0 = Left channel, 1 = Right channel[1]

3. At least one multiplexed data line
   - Officially "serial data (SD)",[1] but can be called SDATA, SDIN, SDOUT, DACDAT, ADCDAT, etc.[2]

It may also include the following lines:

1. Master clock (typically 256 x LRCLK)
   - This is not part of the I2S standard,[4] but is commonly included for synchronizing the internal operation of the analog/digital converters.[3][5]
2. A multiplexed data line for upload

The bit clock pulses once for each discrete bit of data on the data lines. The bit clock frequency is the product of the sample rate, the number of bits per channel and the number of channels. So, for example, CD Audio with a sample frequency of 44.1 kHz, with 16 bits of precision and two channels (stereo) has a bit clock frequency of:

$$44.1\ \text{kHz} \times 16 \times 2 = 1.4112\ \text{MHz}$$

The word select clock lets the device know whether channel 0 or channel 1 is currently being sent, because I²S allows two channels to be sent on the same data line. It is a 50% duty-cycle signal that has the same frequency as the sample frequency. For stereo material, the I²S specification states that left audio is transmitted on the low cycle of the word select clock and the right channel is transmitted on the high cycle. It is typically synchronized to the falling edge of the serial clock, as the data is latched on the rising edge.[1]

Data is signed, encoded as two's complement with the MSB (most significant bit) first.[1] This allows the number of bits per frame to be arbitrary, with no negotiation required between transmitter and receiver.[1]

As an audio interconnect

In audio equipment, I²S is sometimes used as an external link between a CD player and a separate DAC box, as opposed to a purely internal connection within one player box. This may form an alternative to the commonly used AES/EBU or Toslink or S/PDIF standards.

The I²S connection was not intended to be used via cables, and most integrated circuits will not have the correct impedance for coaxial cables. As the impedance adaptation error, associate with the different line length, can cause difference of propagation delay between the clocks line and data line, this can result in synchronization problem between the SCK, WS and data signals, mainly at high sampling frequency and bitrate. As the I²S doesn't have any error detection mechanism, this can cause important decoding error.

There is no standard interconnecting cable for this application. Some manufacturers provide simply three BNC connectors, an 8P8C ("RJ45") socket or a DE-9 connector. Others like Audio Alchemy (now defunct) used DIN connectors. PS Audio, Musica Pristina and Wyred4Sound use an HDMI connector. Dutch manufacturer Van Medevoort has implemented Q-link in some of its equipment, which transfers i2s over 4 RCA connectors (Data, MCK, LRCK, BCK).

See also

- SPI bus
- S/PDIF

References

1. "I²S Specification" (https://web.archive.org/web/20070102004400/http://www.nxp.com/acrobat_download/various/I2SBUS.pdf) (PDF). Philips Semiconductors. June 5, 1996. Archived from the original (http://www.nxp.com/acrobat_download/various/I2SBUS.pdf) (PDF) on January 2, 2007.
2. Lewis, Jerad (January 2012). "Technical Article MS-2275: Common Inter-IC Digital Interfaces for Audio Data Transfer" (http://www.analog.com/media/en/technical-documentation/technical-articles/MS-2275.pdf) (PDF). Analog Devices, Inc.
3. "MCLK in I2S audio protocol" (http://electronics.stackexchange.com/questions/102588/mclk-in-i2s-audio-protocol). *electronics.stackexchange.com*. Retrieved 2016-11-04. "Clock source for the delta-sigma modulators and digital filters. ... It is the clock that is used by the audio codec ... to time and/or drive its own internal operation."
4. "PCM1781 (or any I2S DAC) clock sources - Audio Converters Forum - Audio Converters - TI E2E Community" (https://e2e.ti.com/support/data_converters/audio_converters/f/64/t/504731). *e2e.ti.com*. Retrieved 2016-11-04. "True, the master (modulator) clock is not part of the I2S standard"
5. Arbona, Jorge (September 2010). "Application Report SLAA469 Audio Serial Interface Configurations for Audio Codecs" (http://www.ti.com/lit/an/slaa469/slaa469.pdf) (PDF). "Audio converters based on the delta-sigma (ΔΣ) architecture require an internal master clock that operates at a much faster rate than the target sample rate."

External links

- I²S Specification (https://web.archive.org/web/20070102004400/http://www.nxp.com/acrobat_download/various/I2SBUS.pdf) - Philips/NXP
- I²S and STM32F4 Slides (https://web.archive.org/web/20140223115501/http://www.eng.auburn.edu/~nelson/courses/elec5260_6260/Inter-IC%20Sound%20%28I2S%29%20Bus2.pdf) - Auburn University
- Common inter-IC digital interfaces for audio data transfer (http://www.edn.com/design/consumer/4390981/Common-inter-IC-digital-interfaces-for-audio-data-transfer-), PDF (http://www.analog.com/static/imported-files/tech_articles/MS-2275.pdf)