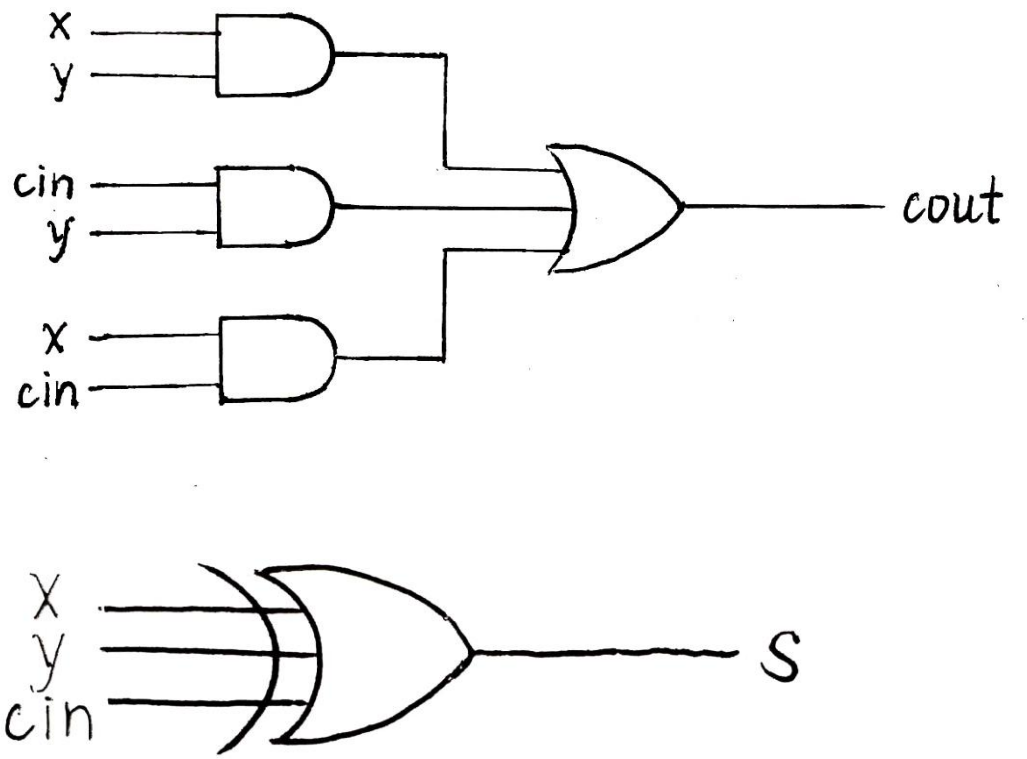
1. Emulate exp1 in lab1 (a full adder s+cout=x+y+cin) with the following parameters.

1.1 I/O:

I/O	x	y	cin	s	cout
LOC	V17	V16	W16	U16	E19

1.2 Circuit Diagram:

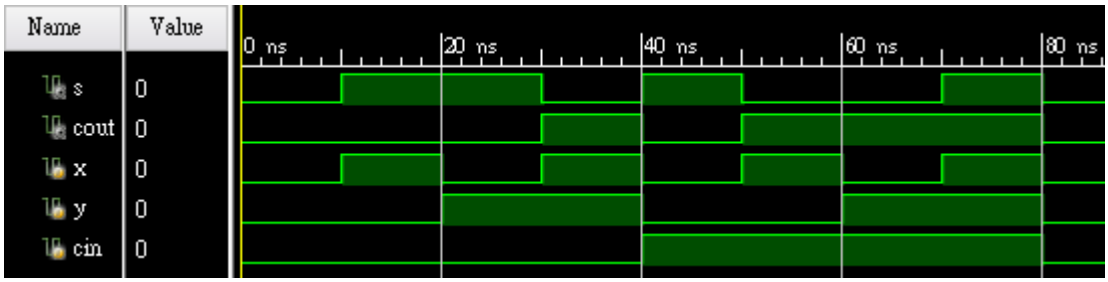


1.3 Verilog HDL Coding:

```
23 module fulladder(
24     output s,      //sum
25     output cout,   //carry out
26     input  x,      //augend
27     input  y,      //addend
28     input  cin     //carry in
29     );
30
31     assign {cout, s} = x + y + cin;
32
33 endmodule         //fulladder
```

1.4 Testbench Verification:

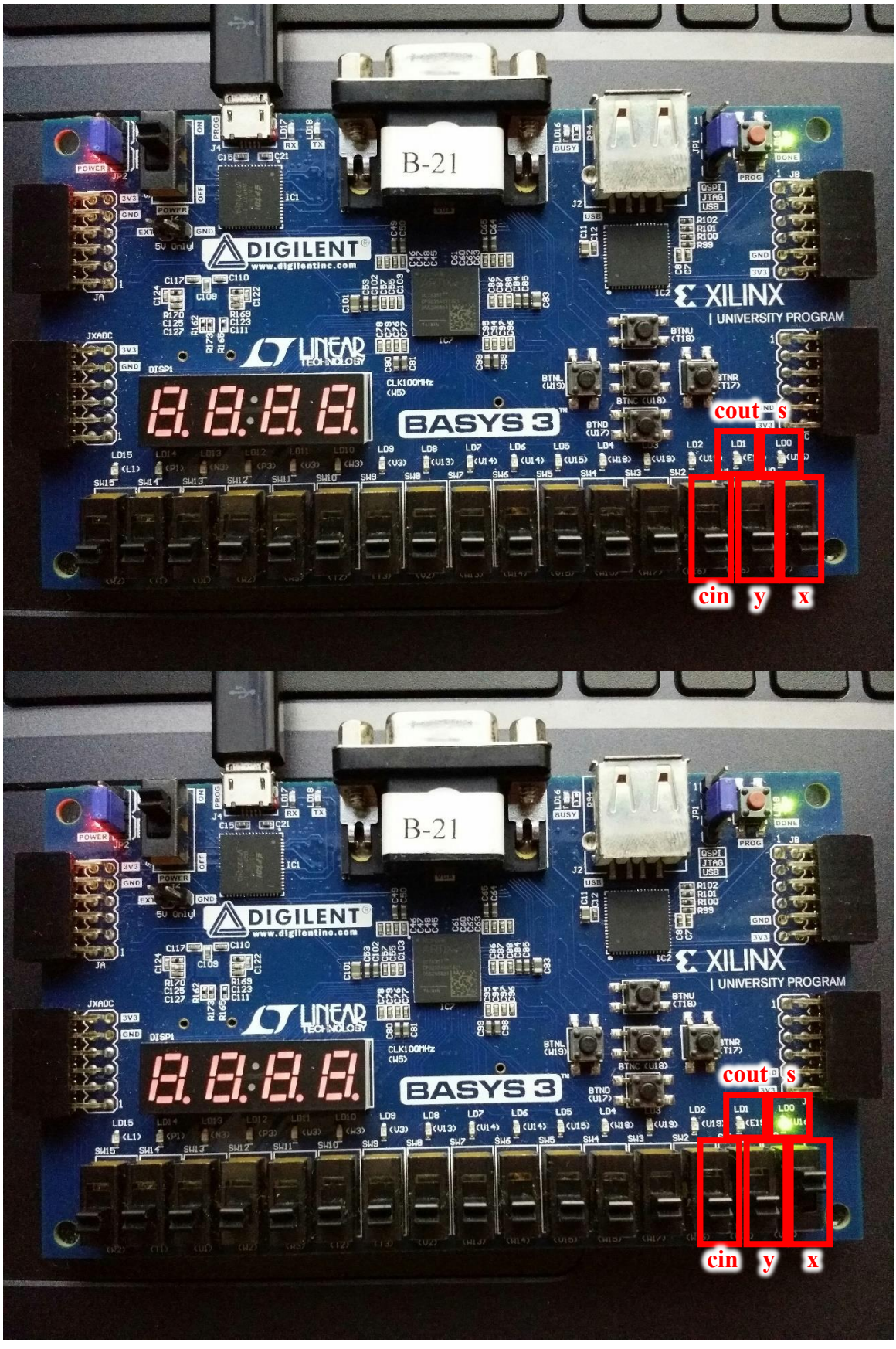
```
23  module fulladder_test();
24      // output
25      wire s;      // sum
26      wire cout;   // carry out
27
28      // input
29      reg  x;      // augend
30      reg  y;      // addend
31      reg  cin;    // carry in
32
33      // instantiate
34      fulladder DUT(
35          .s(s),          // sum
36          .cout(cout),    // carry out
37          .x(x),          // augend
38          .y(y),          // addend
39          .cin(cin)       // carry in
40          );
41
42      // stimulus
43      initial    {cin, y, x} = 0;
44      always #10 {cin, y, x} = {cin, y, x} + 1;
45
46  endmodule        // fulladder_test
```

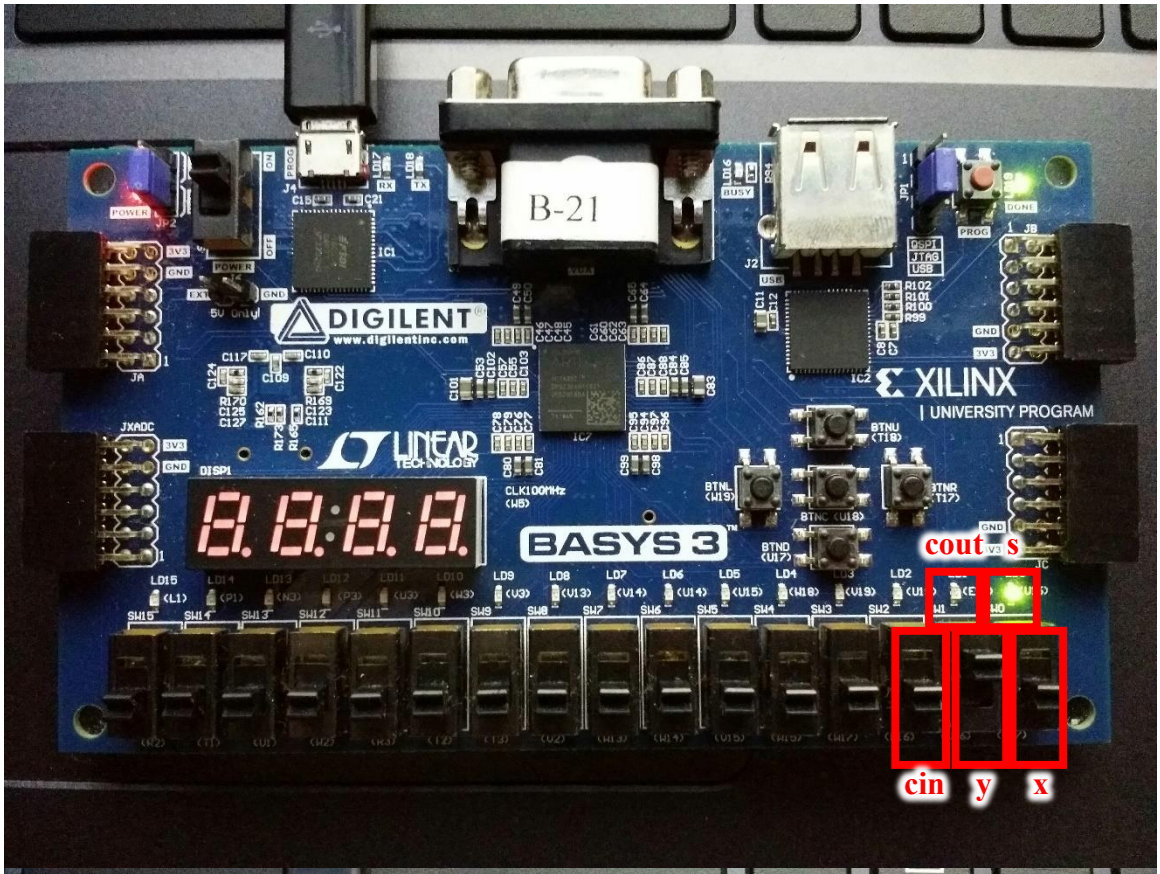


1.5 I/O Pins Assignment:

Name	Direction	Package Pin	I/O Std
All ports (5)			
Scalar ports (5)			
cin	IN	W16	LVCMOS33*
cout	OUT	E19	LVCMOS33*
s	OUT	U16	LVCMOS33*
x	IN	V17	LVCMOS33*
y	IN	V16	LVCMOS33*

1.6 Synthesis and Implementation:

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y
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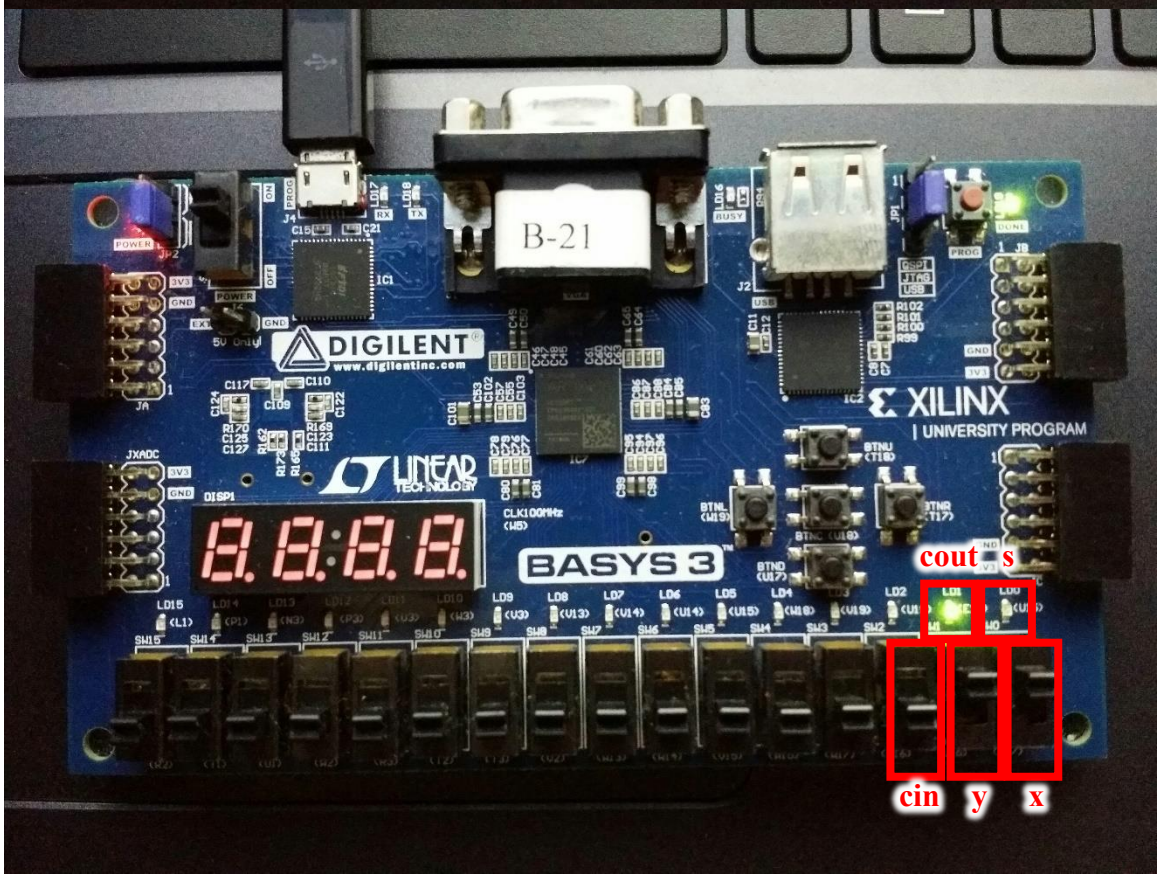
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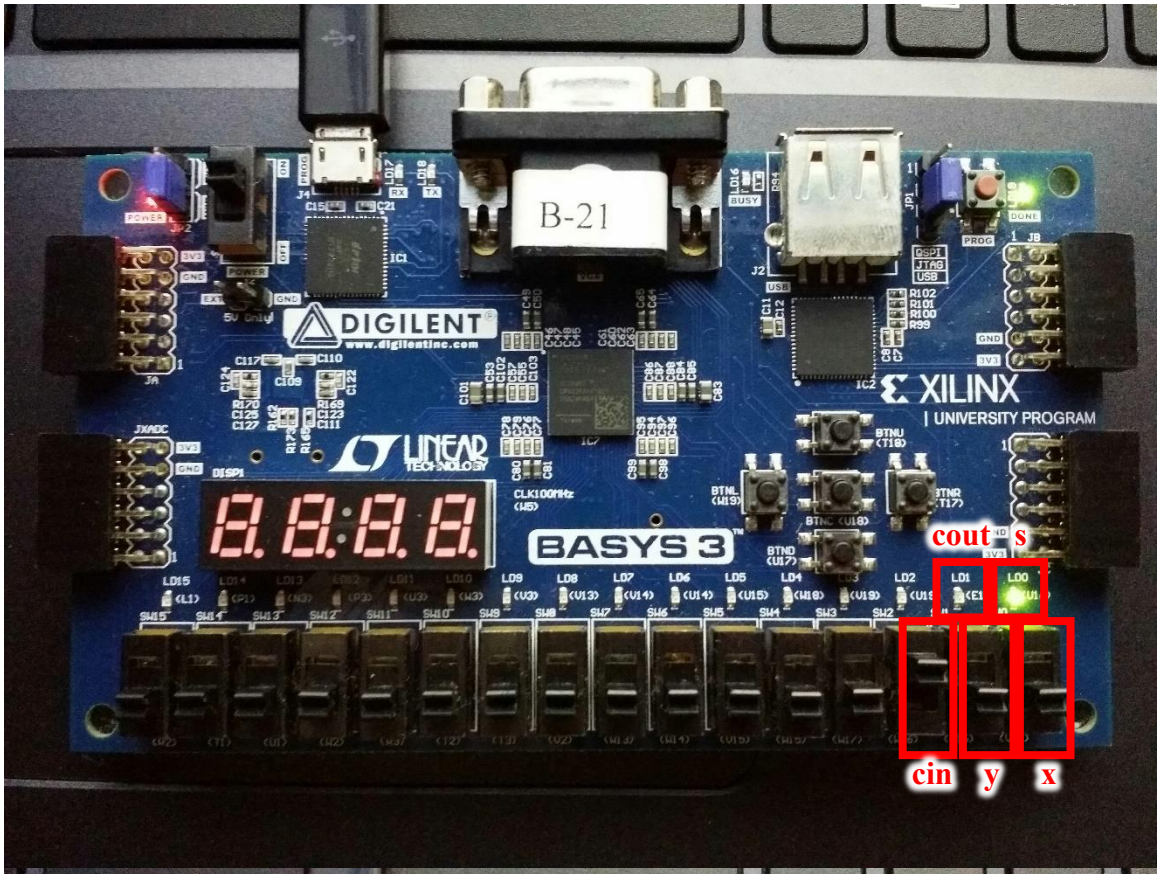
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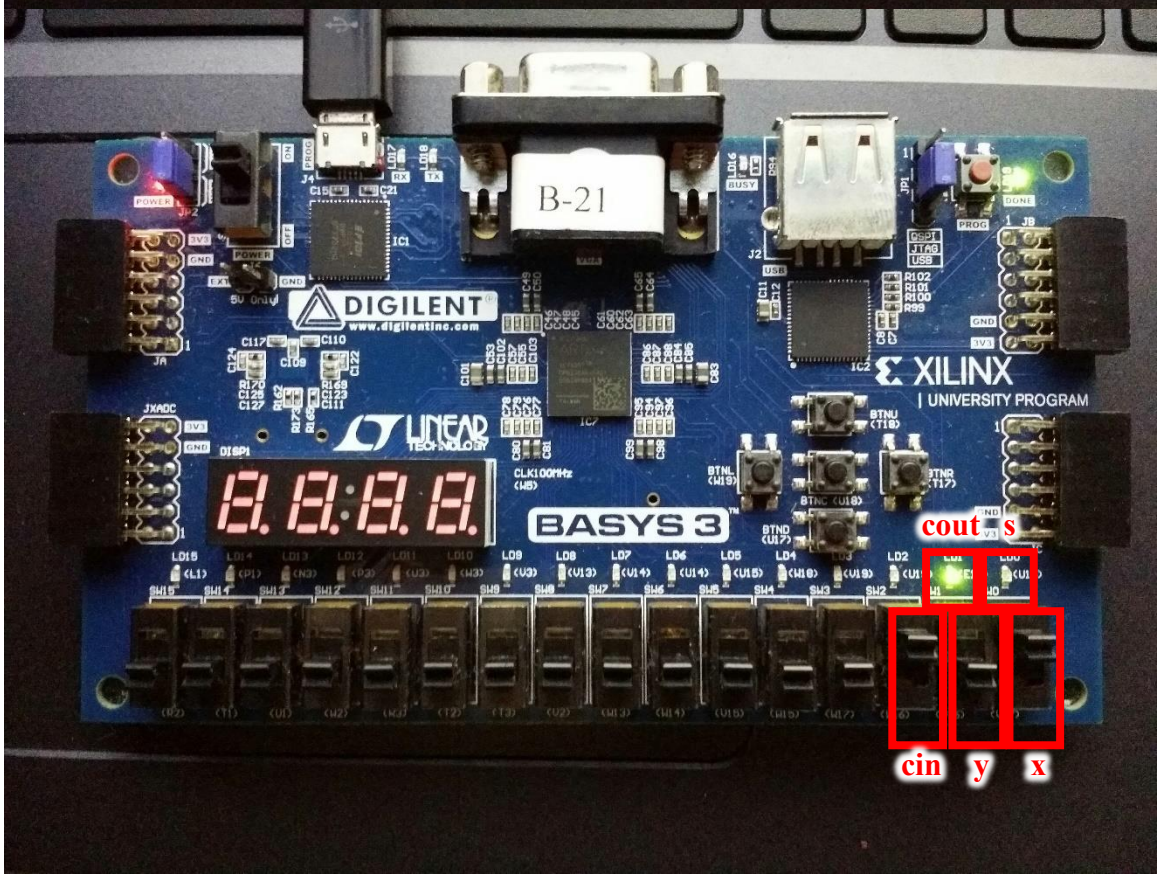
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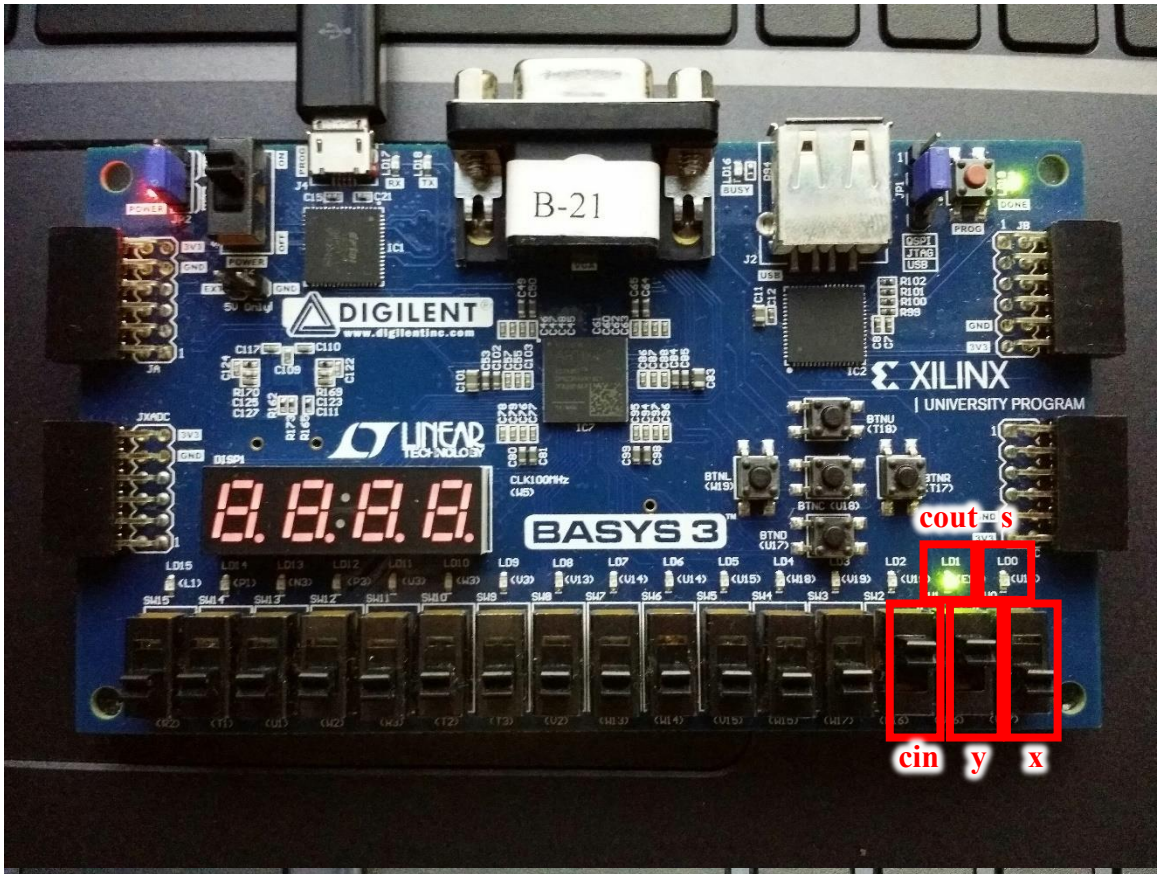
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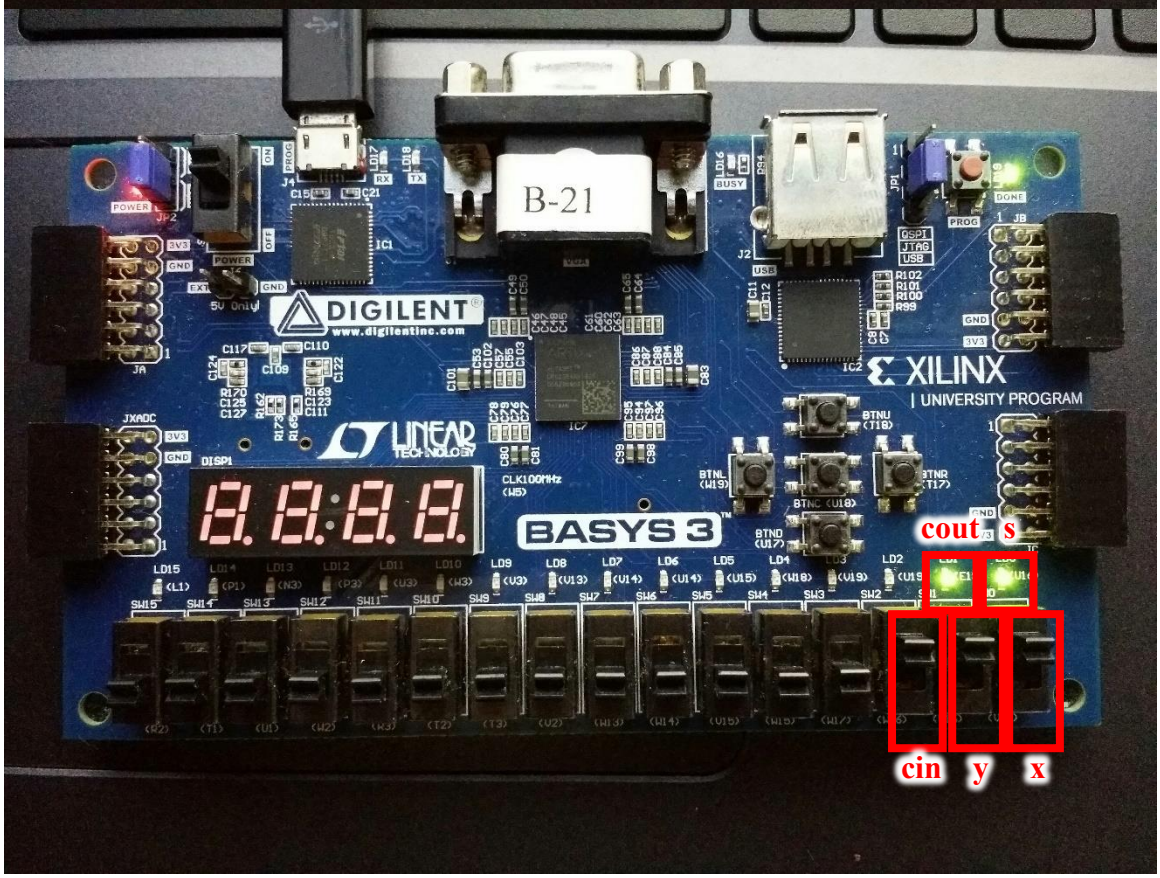
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2. Derive a BCD (i[3:0]) to 7-segment display decoder (D_ssd[7:0]), and also use four LEDs (d[3:0]) to monitor the 4-bit BCD number. (Other values of i outside the range will show F).

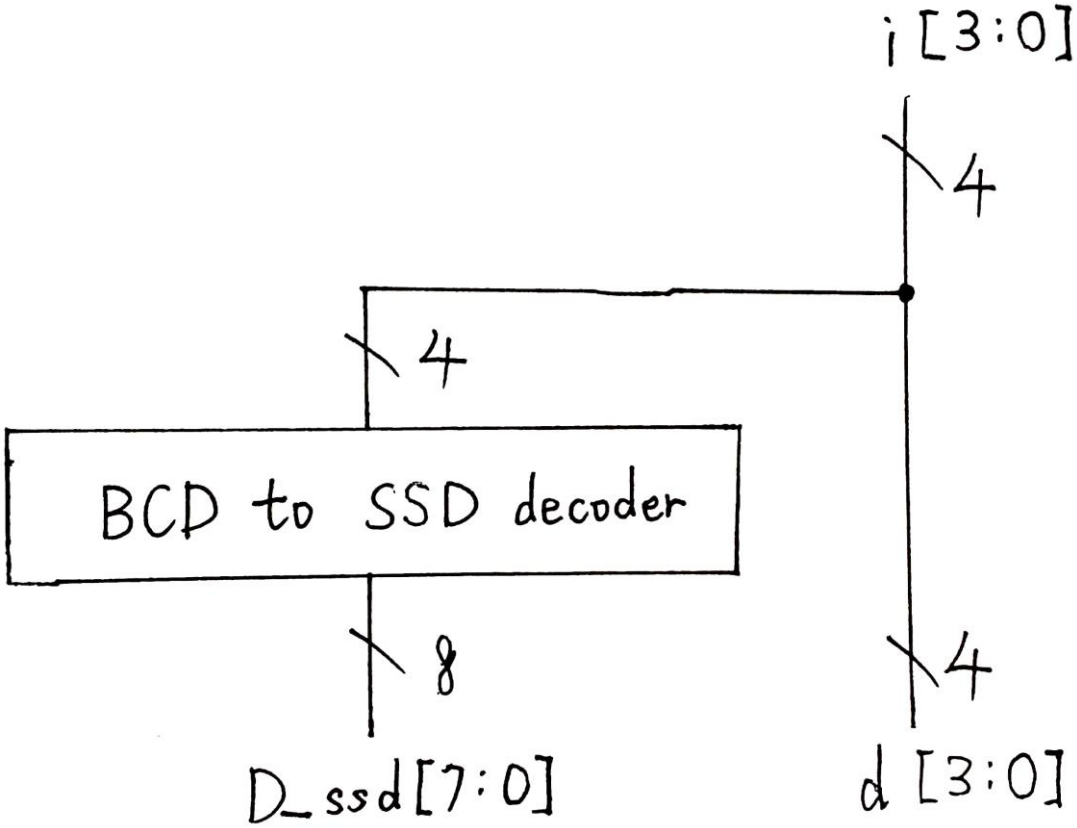
2.1 I/O:

inputs: i[3:0]

outputs: D_ssd[7:0]

d[3:0]

2.2 Circuit Diagram:

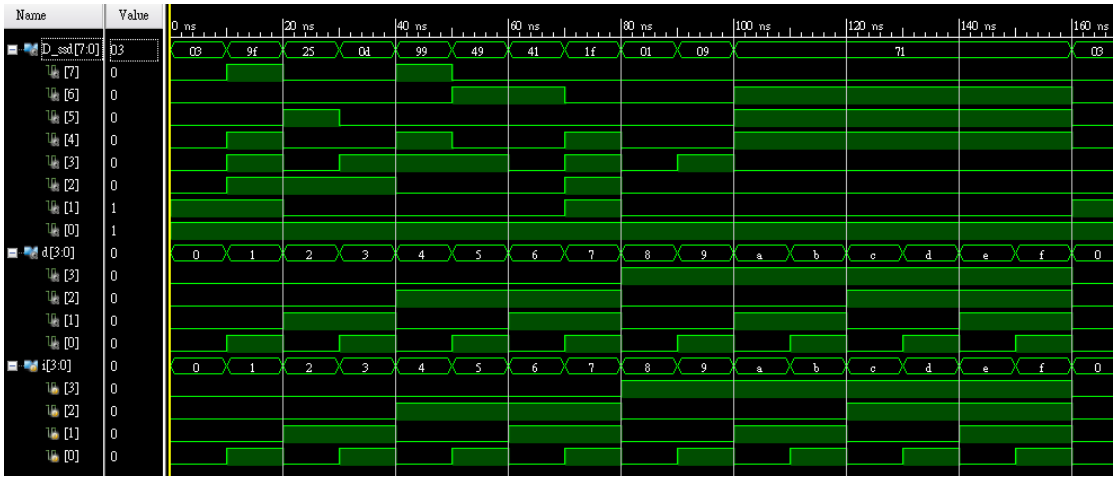


2.3 Verilog HDL Coding:

```
23 module BCD_to_SSD_decoder(
24     output reg [7:0] D_ssd,  // 7-segment display decode
25     output     [3:0] d,      // LEDs to monitor
26     input      [3:0] i       // 4-bit BCD number
27     );
28
29     // four LEDs to monitor the 4-bit BCD number
30     assign d = i;
31
32     // BCD to 7-segment display decoder
33     always @ (i)
34     begin
35         case (i)
36             0:       D_ssd = 8'b0000001_1;  // 0
37             1:       D_ssd = 8'b1001111_1;  // 1
38             2:       D_ssd = 8'b0010010_1;  // 2
39             3:       D_ssd = 8'b0000110_1;  // 3
40             4:       D_ssd = 8'b1001100_1;  // 4
41             5:       D_ssd = 8'b0100100_1;  // 5
42             6:       D_ssd = 8'b0100000_1;  // 6
43             7:       D_ssd = 8'b0001111_1;  // 7
44             8:       D_ssd = 8'b0000000_1;  // 8
45             9:       D_ssd = 8'b0000100_1;  // 9
46             default: D_ssd = 8'b0111000_1;  // F
47         endcase
48     end
49
50 endmodule                    // BCD_to_SSD_decoder
```

2.4 Testbench Verification:

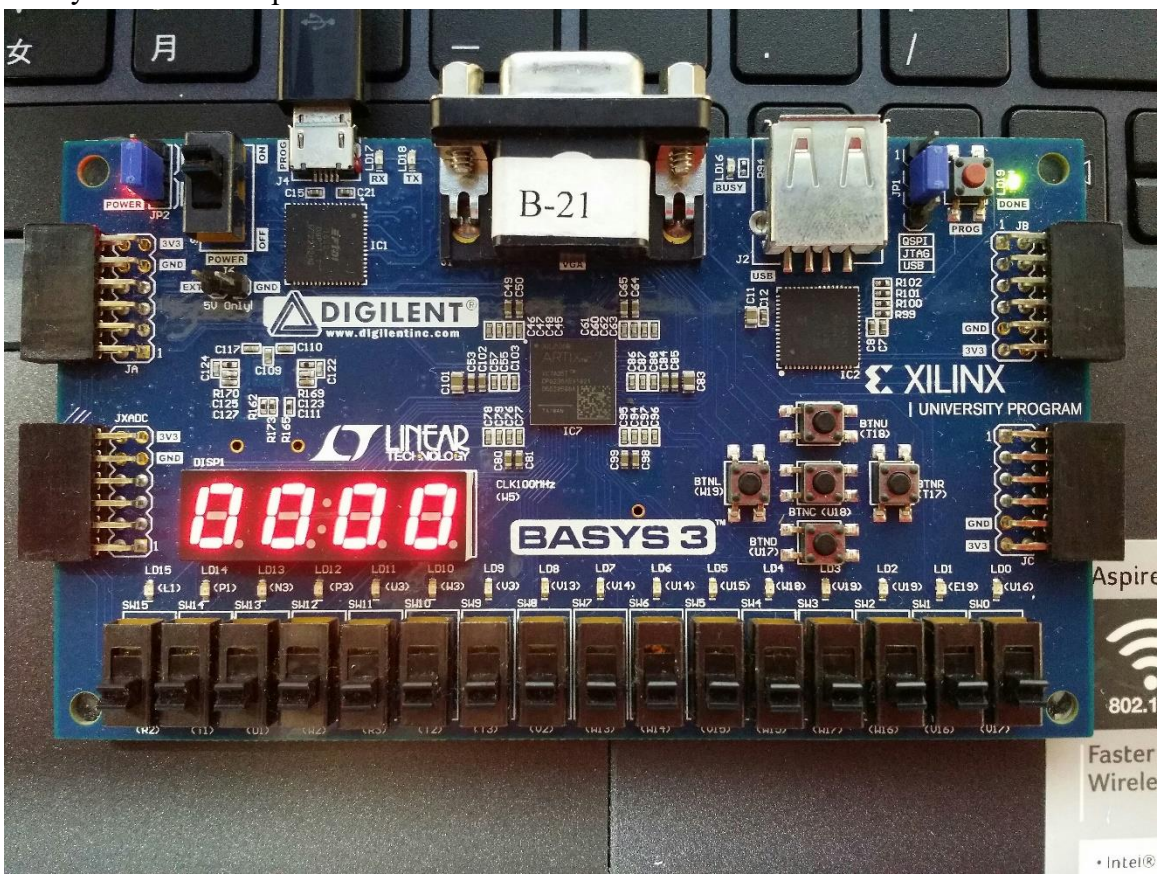
```
23  module BCD_to_SSD_decoder_test();
24      // output
25      wire [7:0] D_ssd;   // 7-segment display decode
26      wire [3:0] d;       // LEDs to monitor
27
28      // input
29      reg  [3:0] i;       // 4-bit BCD number
30
31      // instantiate
32      BCD_to_SSD_decoder DUT(
33          .D_ssd(D_ssd),  // 7-segment display decode
34          .d(d),          // four LEDs to monitor the 4-bit BCD number
35          .i(i)           // 4-bit BCD number
36          );
37
38      // stimulus
39      initial
40          i = 0;
41      always
42          #10 i = i + 1;
43
44  endmodule               // BCD_to_SSD_decoder_test
```

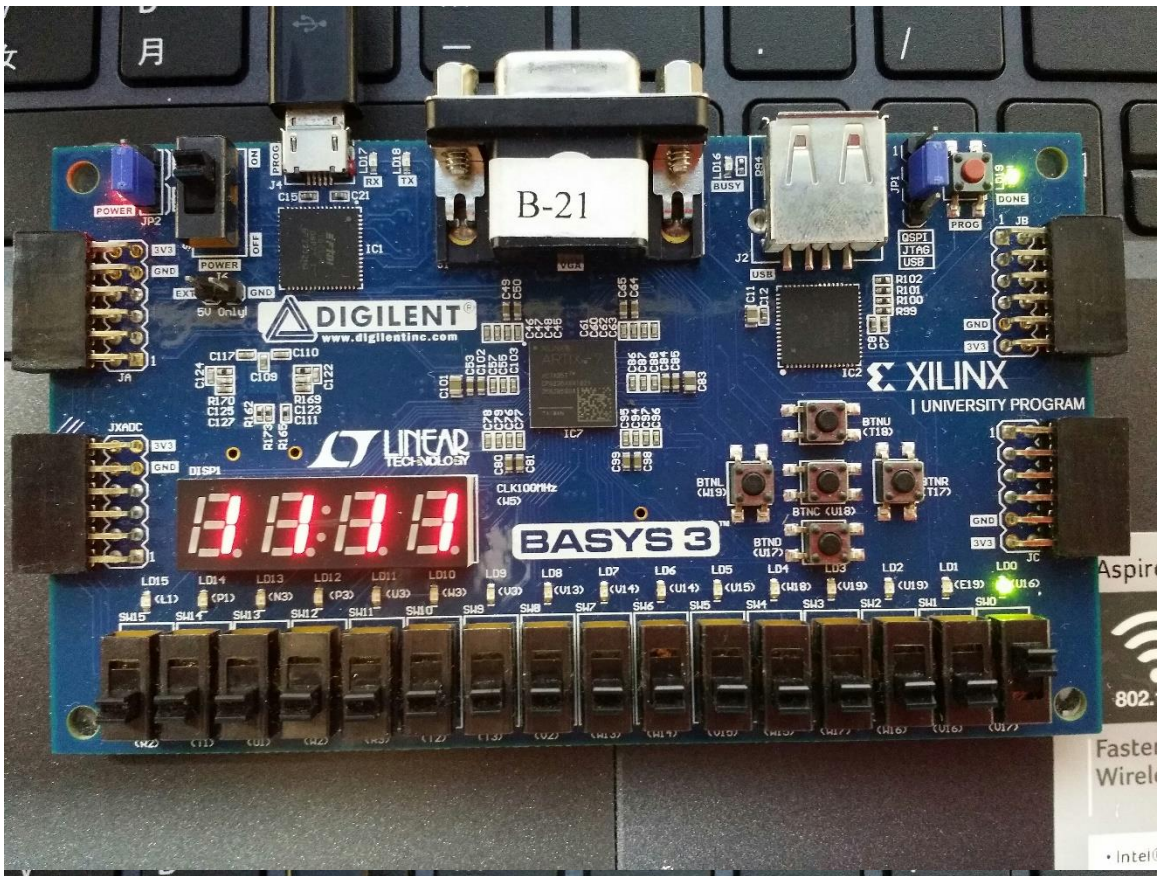


2.5 I/O Pins Assignment

Name	Direction	Package Pin	I/O Std
All ports (16)			
d (4)	OUT		LVCMOS33*
d[3]	OUT	V19	LVCMOS33*
d[2]	OUT	U19	LVCMOS33*
d[1]	OUT	E19	LVCMOS33*
d[0]	OUT	U16	LVCMOS33*
D_ssd (8)	OUT		LVCMOS33*
D_ssd[7]	OUT	W7	LVCMOS33*
D_ssd[6]	OUT	W6	LVCMOS33*
D_ssd[5]	OUT	U8	LVCMOS33*
D_ssd[4]	OUT	V8	LVCMOS33*
D_ssd[3]	OUT	U5	LVCMOS33*
D_ssd[2]	OUT	V5	LVCMOS33*
D_ssd[1]	OUT	U7	LVCMOS33*
D_ssd[0]	OUT	V7	LVCMOS33*
i (4)	IN		LVCMOS33*
i[3]	IN	W17	LVCMOS33*
i[2]	IN	W16	LVCMOS33*
i[1]	IN	V16	LVCMOS33*
i[0]	IN	V17	LVCMOS33*

2.6 Synthesis and Implementation:

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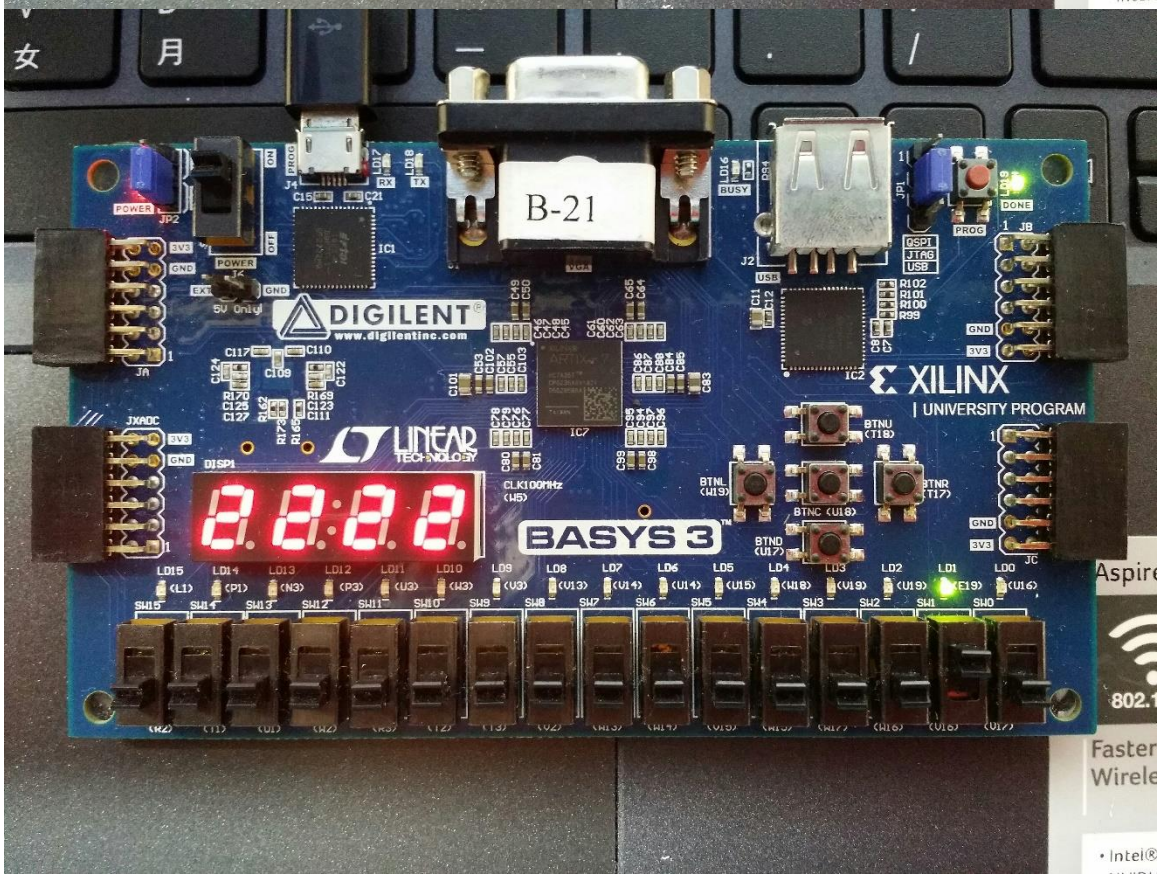
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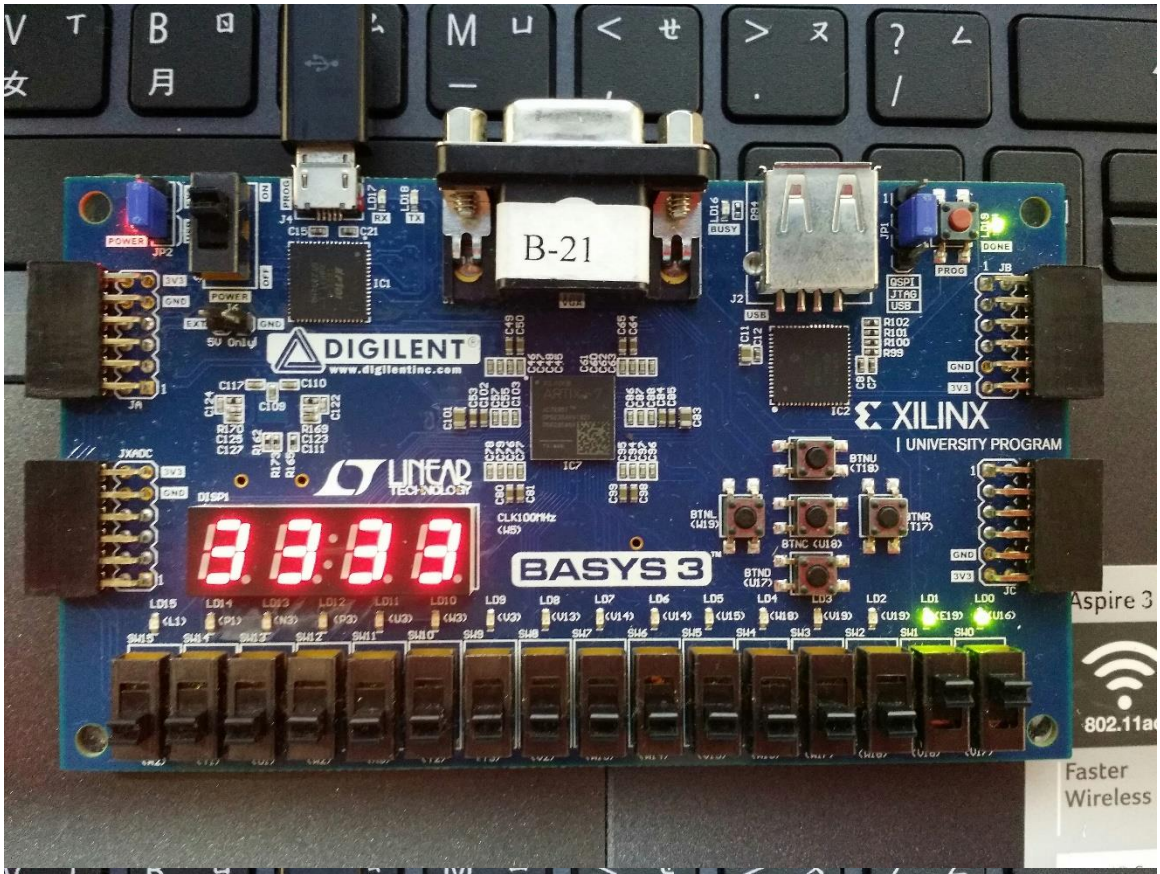
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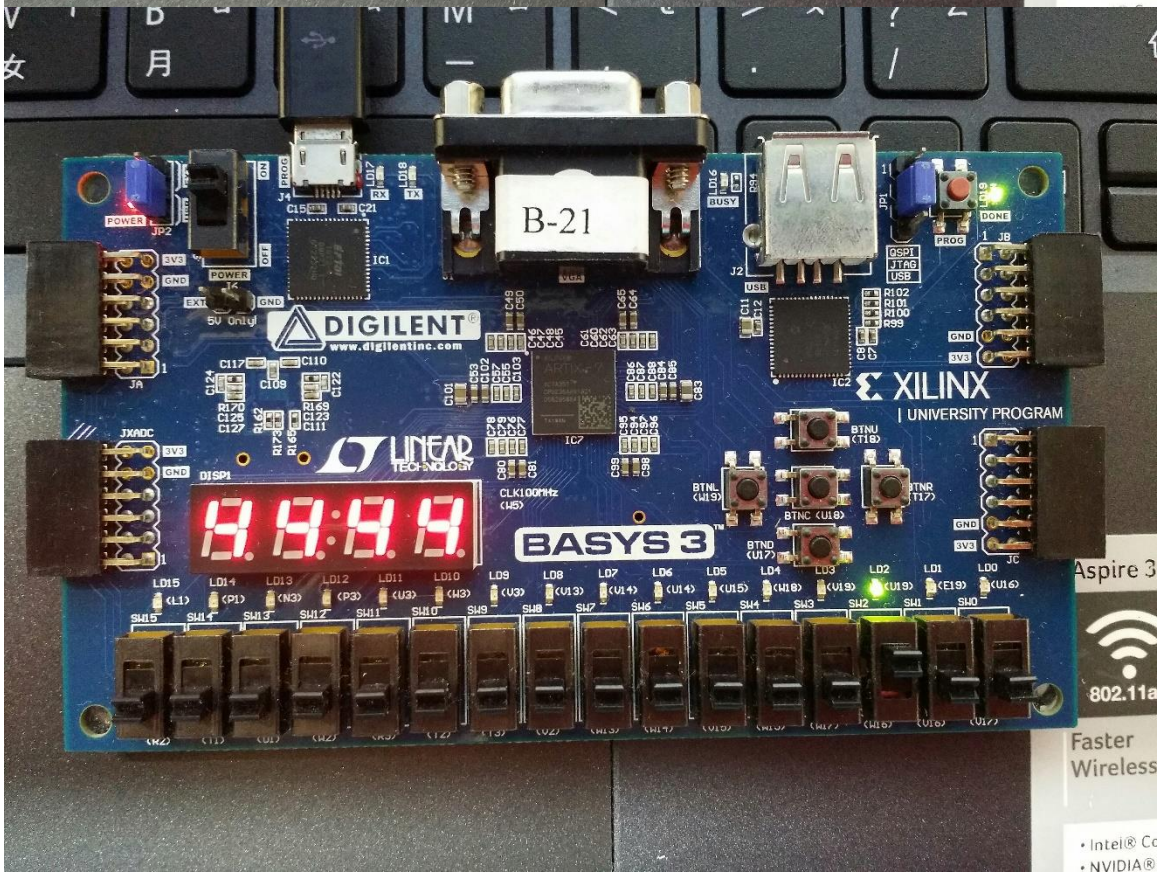
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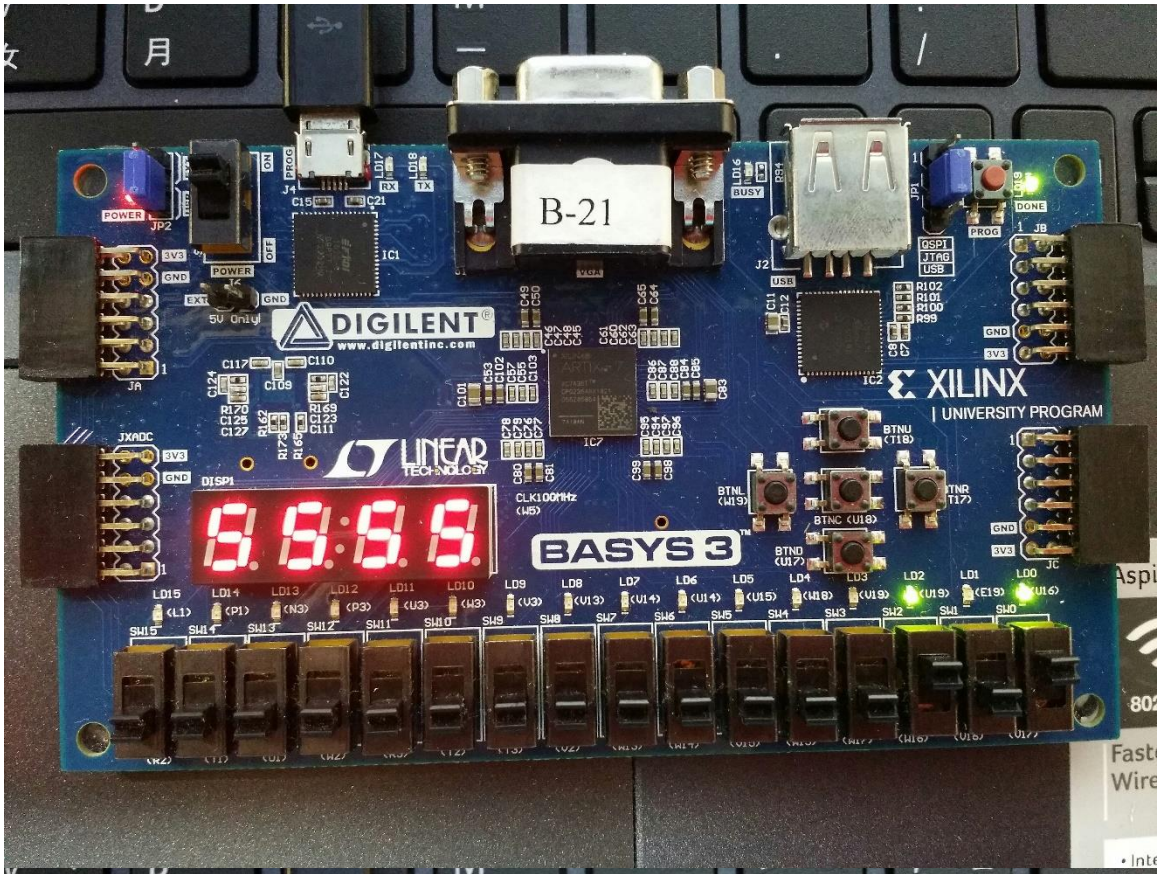
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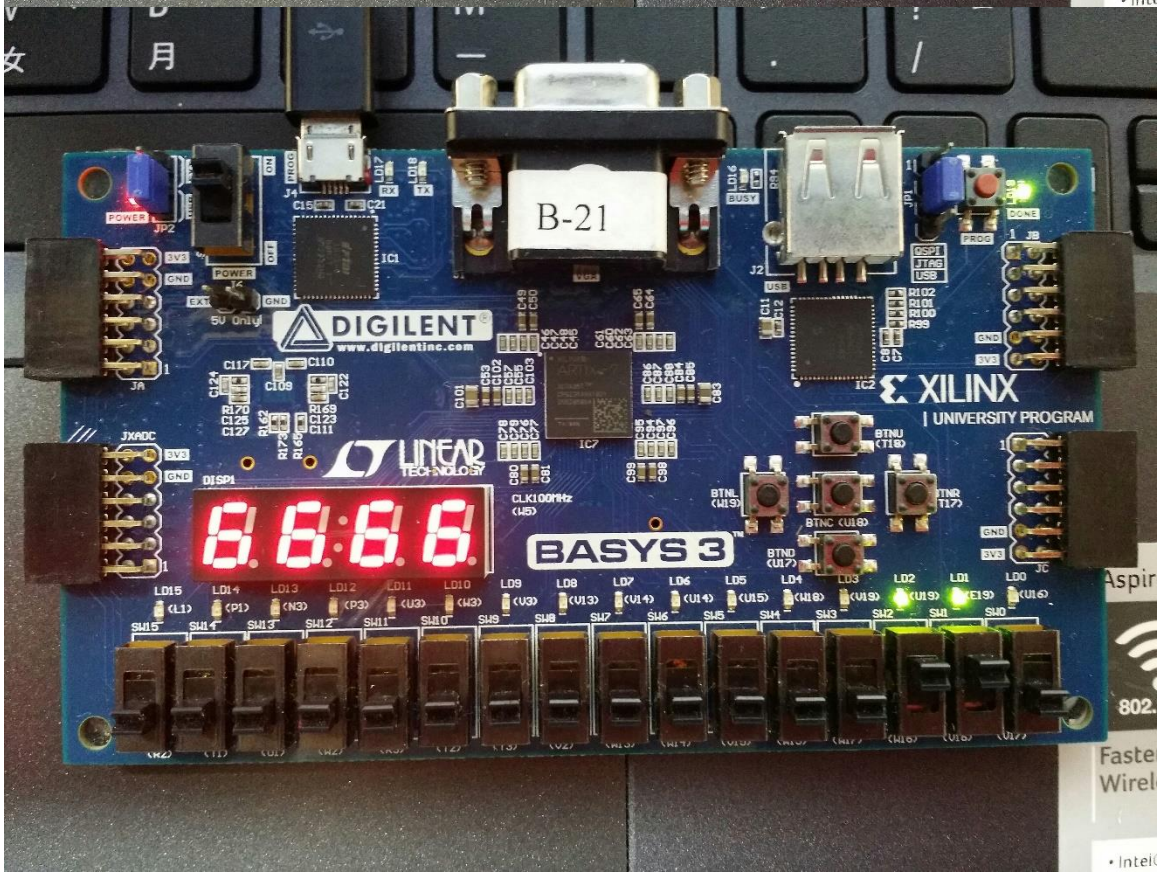
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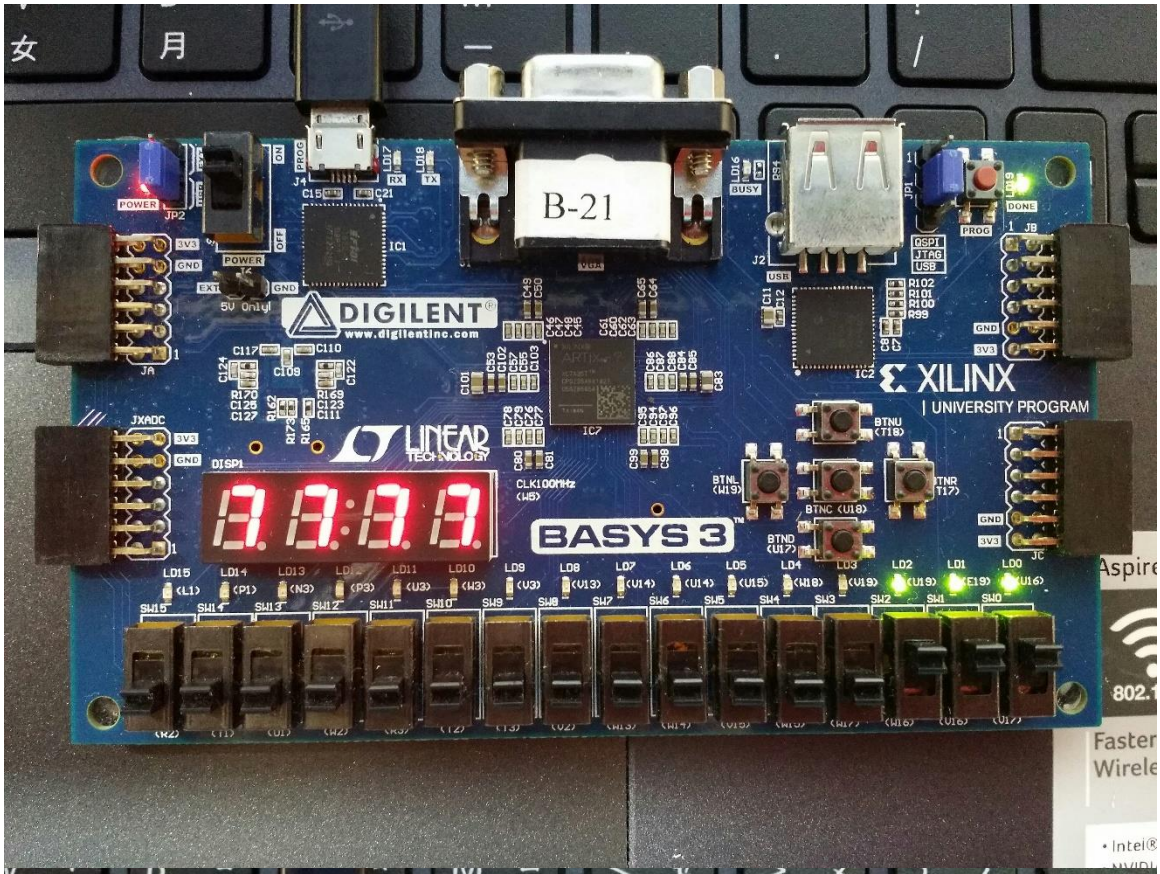
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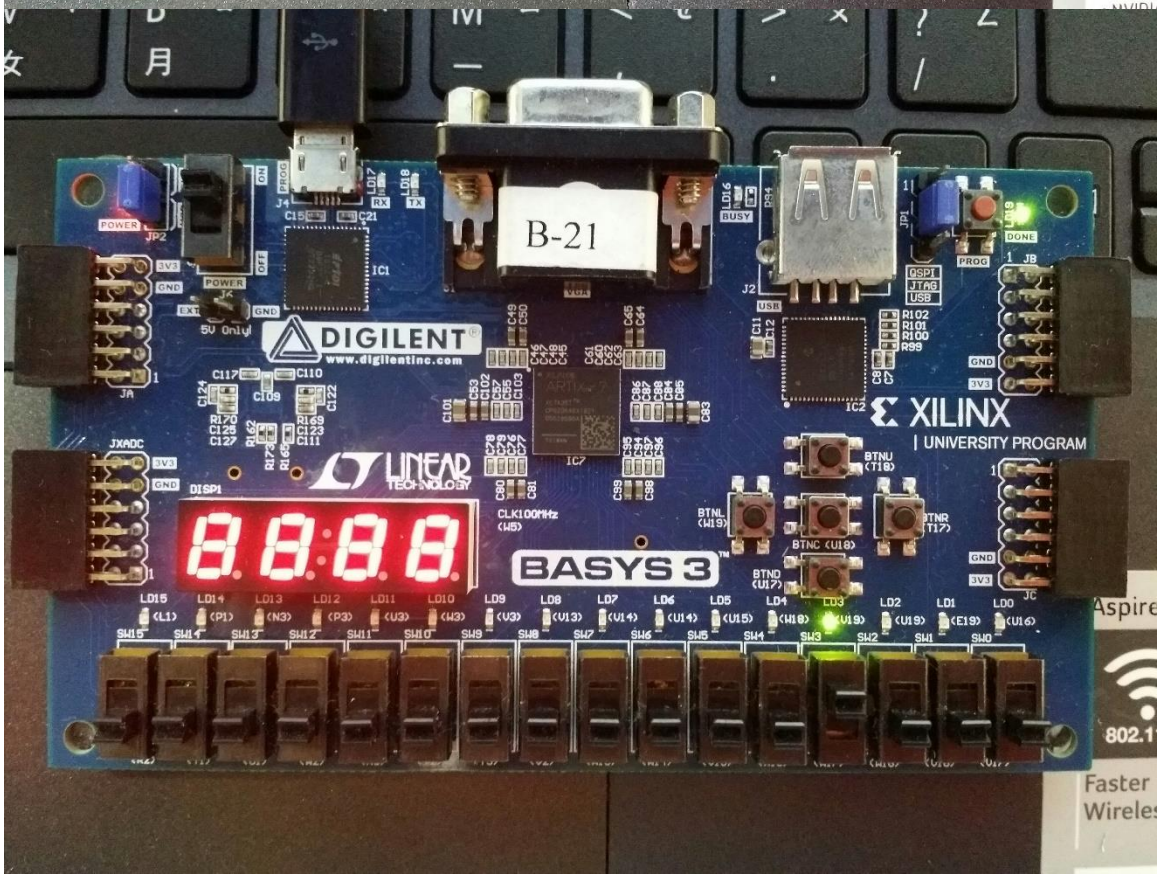
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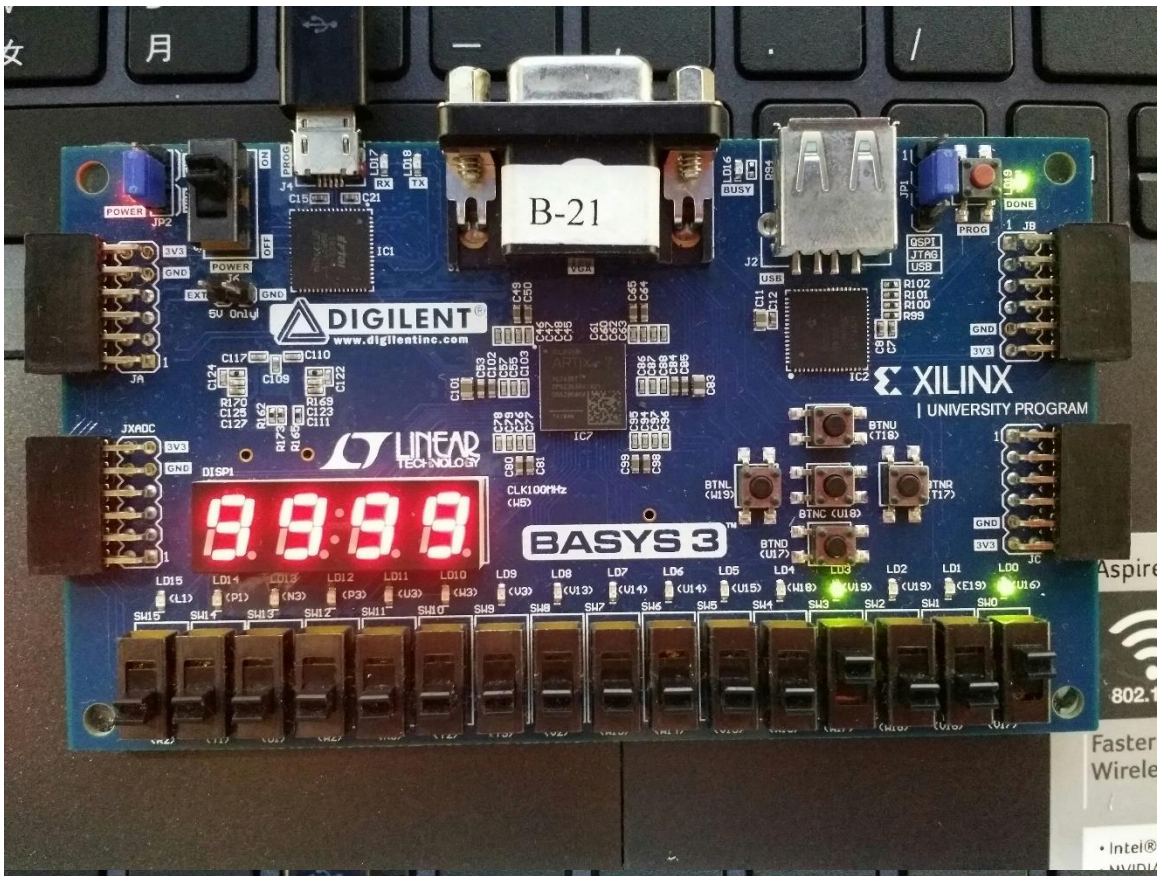
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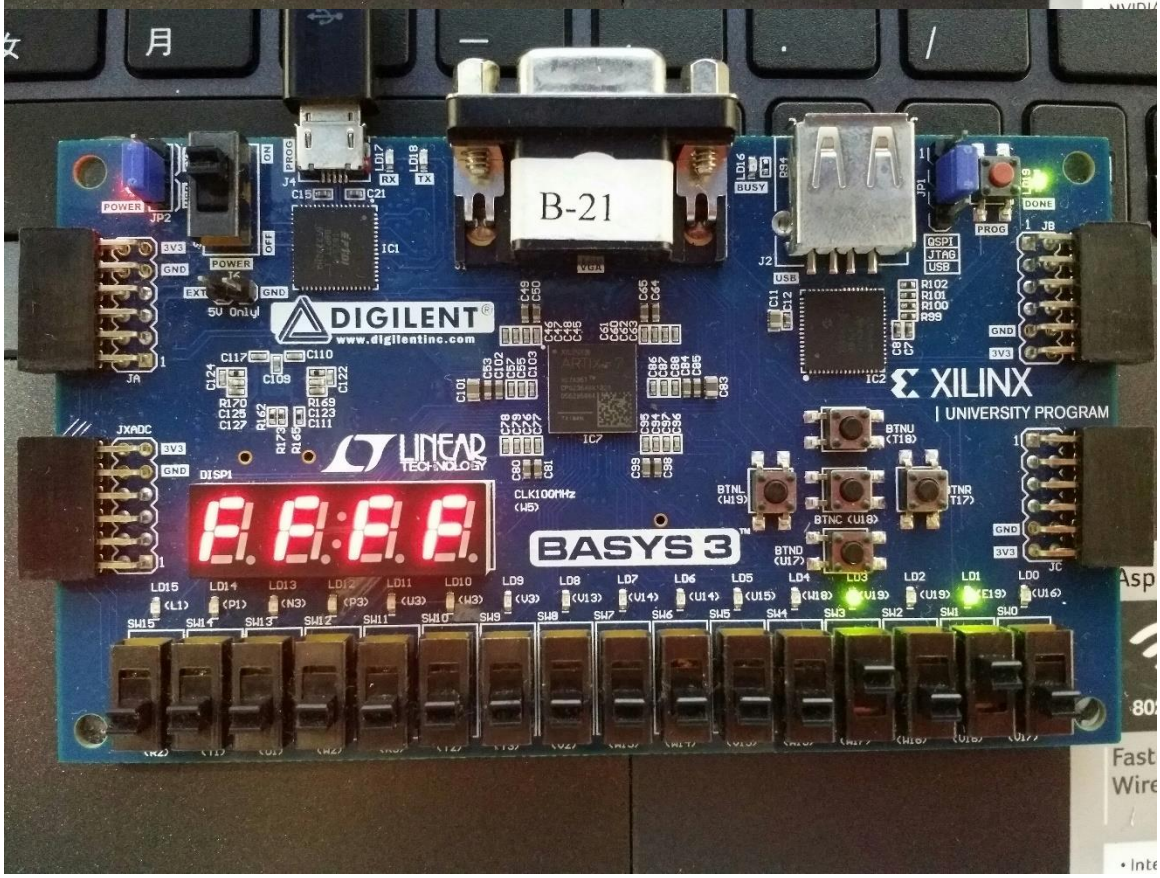
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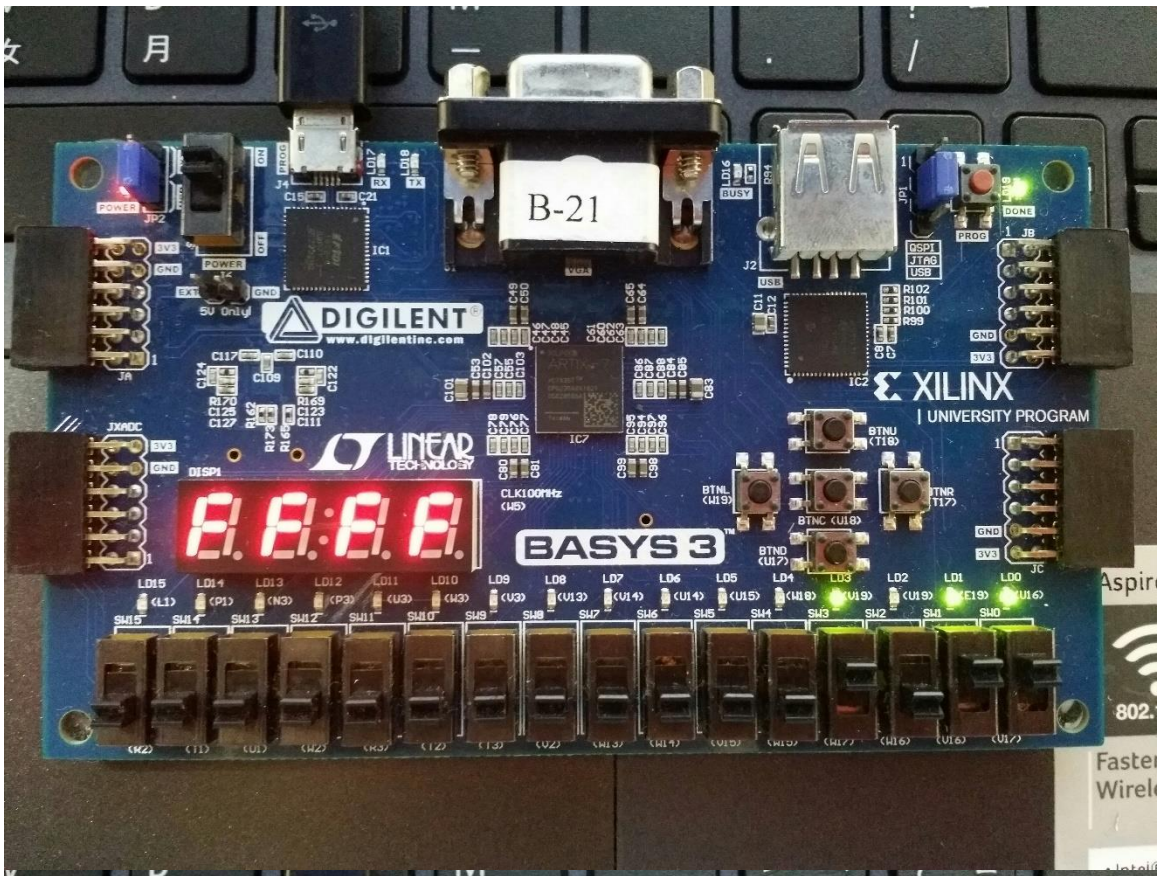
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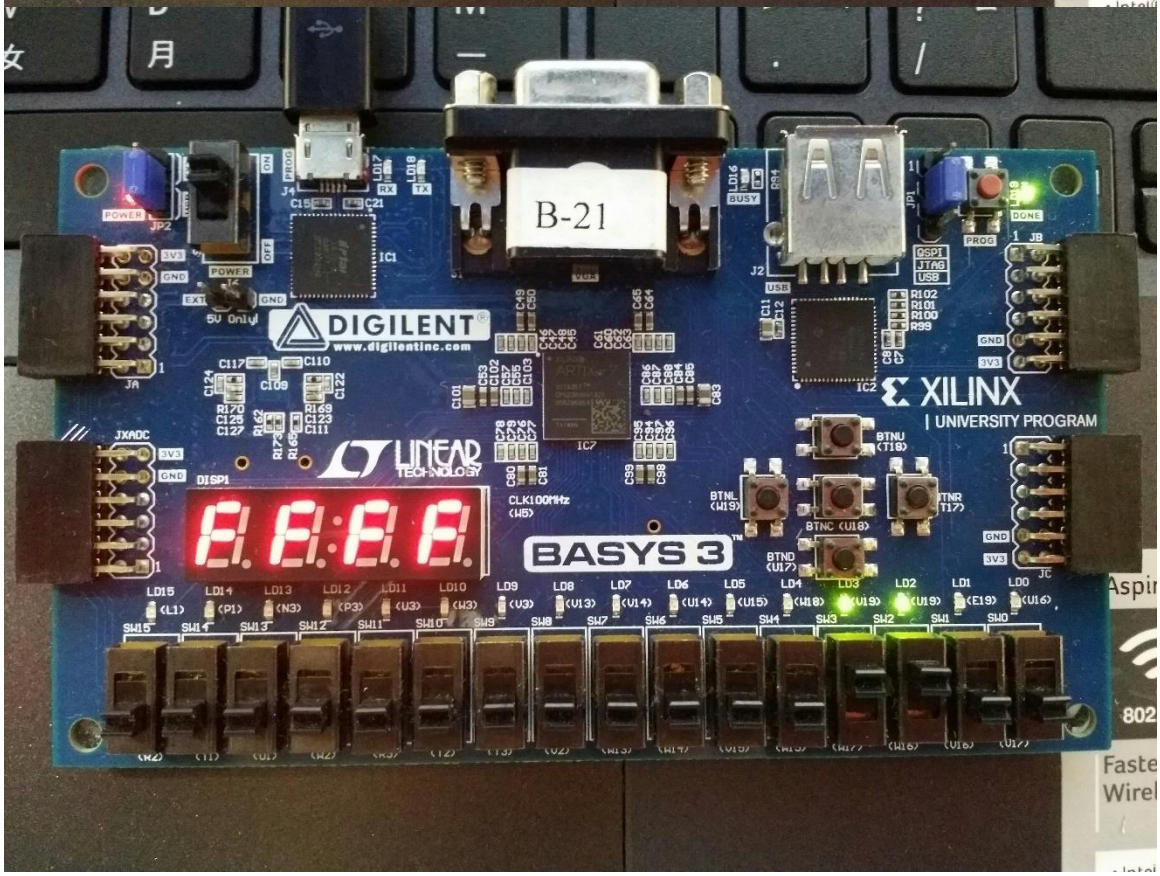
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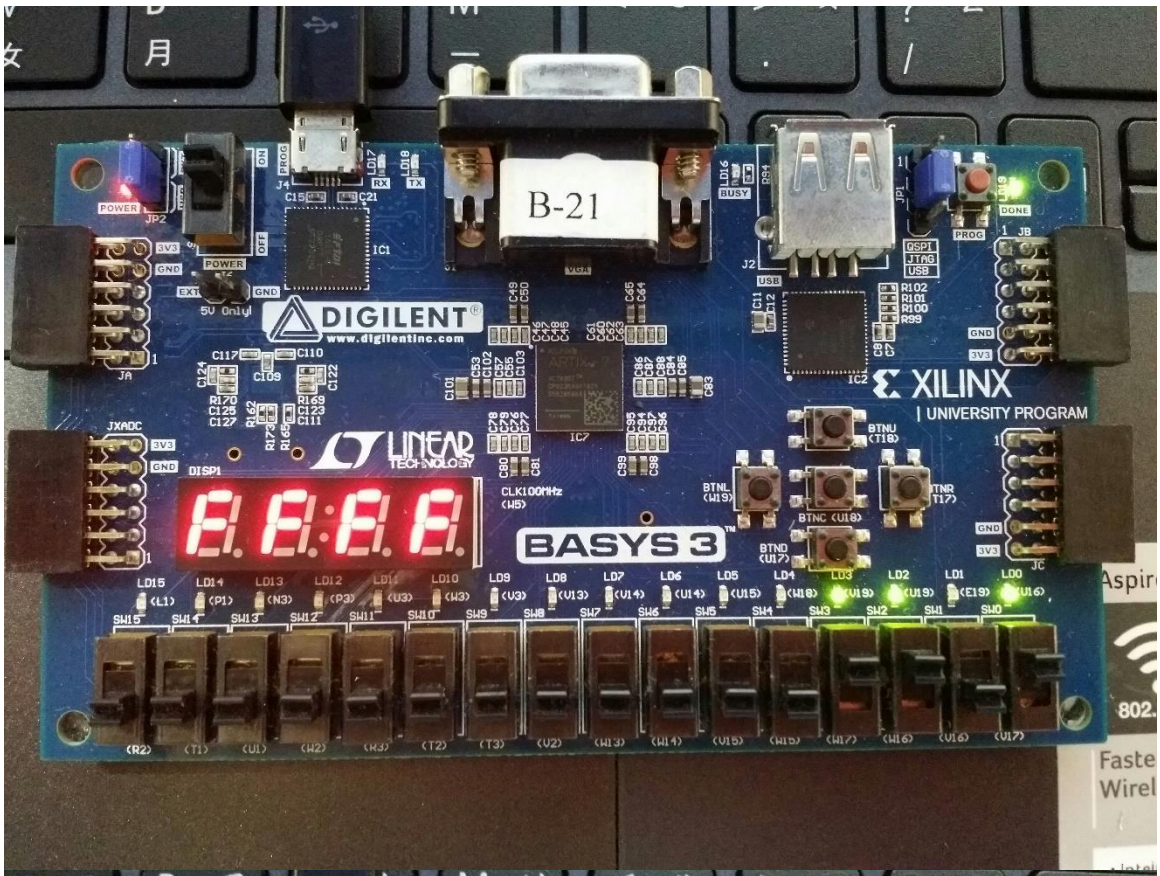
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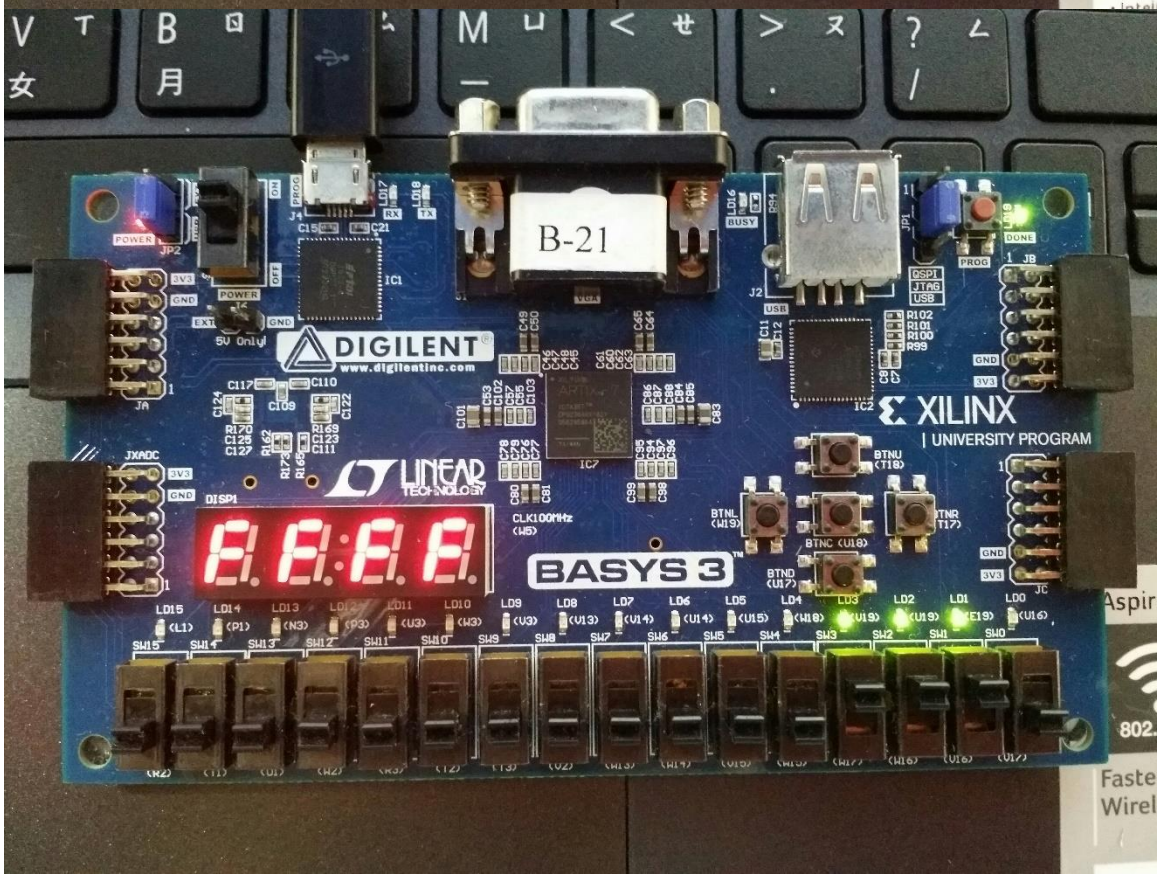
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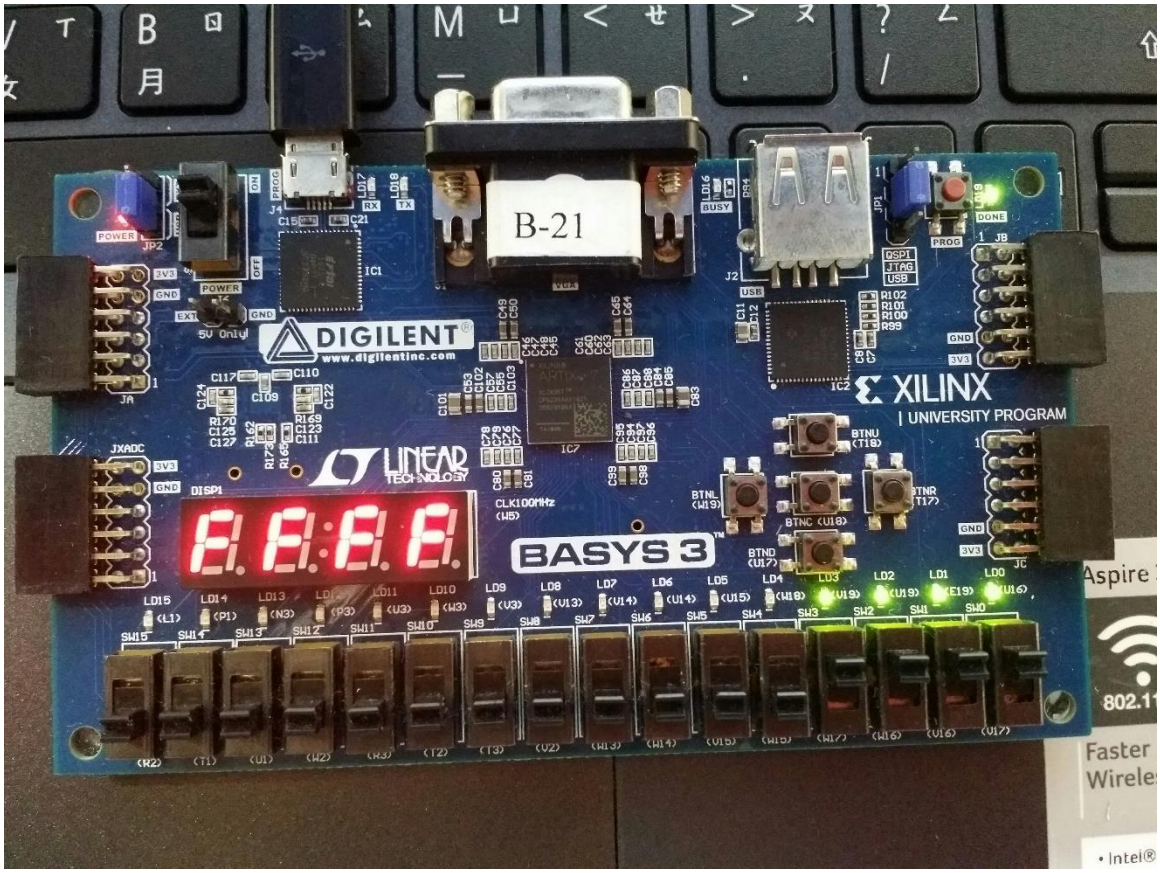
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SW15 SW14 SW13 SW12 SW11 SW10 SW9 SW8 SW7 SW6 SW5 SW4 SW3 SW2 SW1 SW0
POWER
PROG
DONE
QSPI
JTAG
USB
5V Only

3. Derive a binary (i[3:0], 0-9, a, b, c, d, e, f) to 7-segment display decoder (D[7:0]), and also use four LEDs (d[3:0]) to monitor the 4-bit binary number.

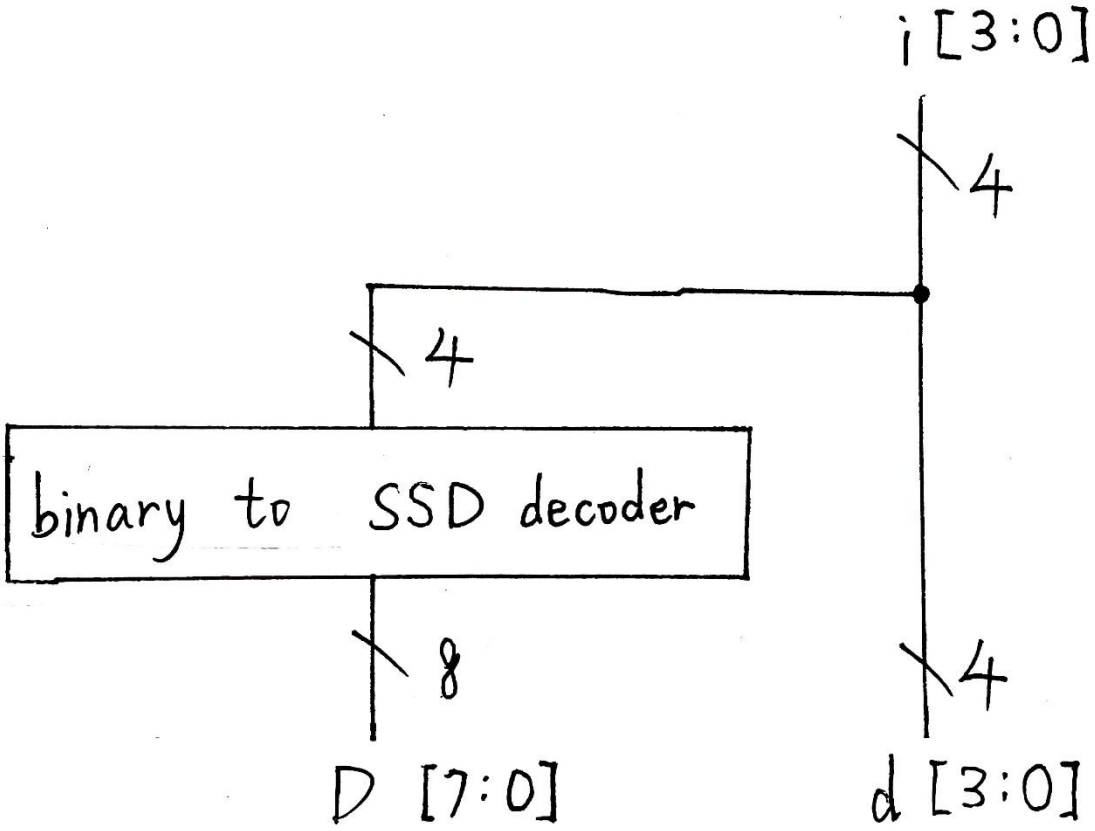
3.1 I/O:

inputs: i[3:0]

outputs: D[7:0]

d[3:0]

3.2 Circuit Diagram:

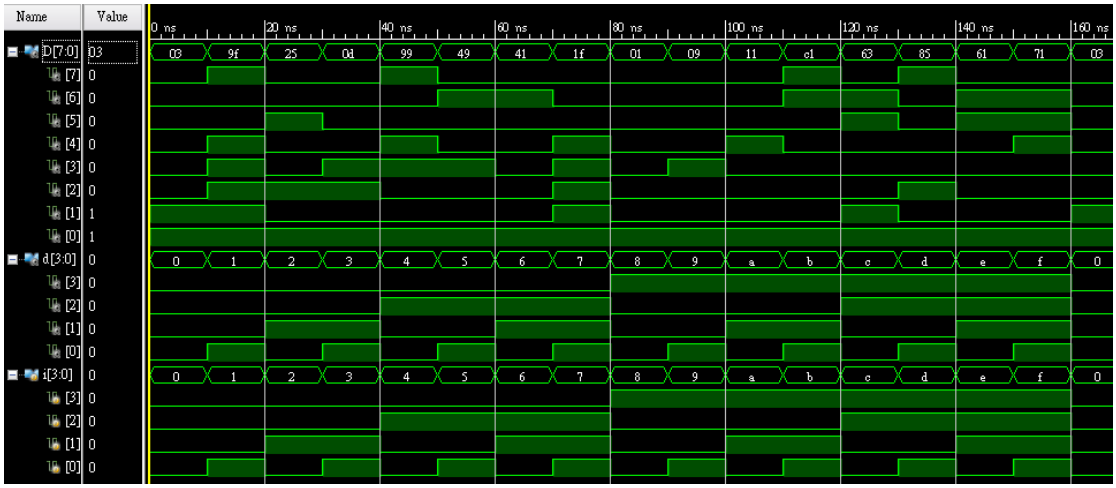


3.3 Verilog HDL Coding:

```
23  module binary_to_SSD_decoder(
24      output reg [7:0] D,       // 7-segment display decode
25      output     [3:0] d,       // LEDs to monitor
26      input      [3:0] i        // 4-bit binary number
27      );
28
29      // use four LEDs to monitor the 4-bit binary number
30      assign d = i;
31
32      // binary (0-9, a, b, c, d, e, f) to 7-segment display decoder
33      always @ (i)
34      begin
35          case (i)
36              0:       D = 8'b0000001_1;  // 0
37              1:       D = 8'b1001111_1;  // 1
38              2:       D = 8'b0010010_1;  // 2
39              3:       D = 8'b0000110_1;  // 3
40              4:       D = 8'b1001100_1;  // 4
41              5:       D = 8'b0100100_1;  // 5
42              6:       D = 8'b0100000_1;  // 6
43              7:       D = 8'b0001111_1;  // 7
44              8:       D = 8'b0000000_1;  // 8
45              9:       D = 8'b0000100_1;  // 9
46              10:      D = 8'b0001000_1;  // a
47              11:      D = 8'b1100000_1;  // b
48              12:      D = 8'b0110001_1;  // c
49              13:      D = 8'b1000010_1;  // d
50              14:      D = 8'b0110000_1;  // e
51              15:      D = 8'b0111000_1;  // f
52              default: D = 8'b0111000_1;  // f
53          endcase
54      end                         // always
55
56  endmodule                       // binary_to_SSD_decoder
```

3.4 Testbench Verification:

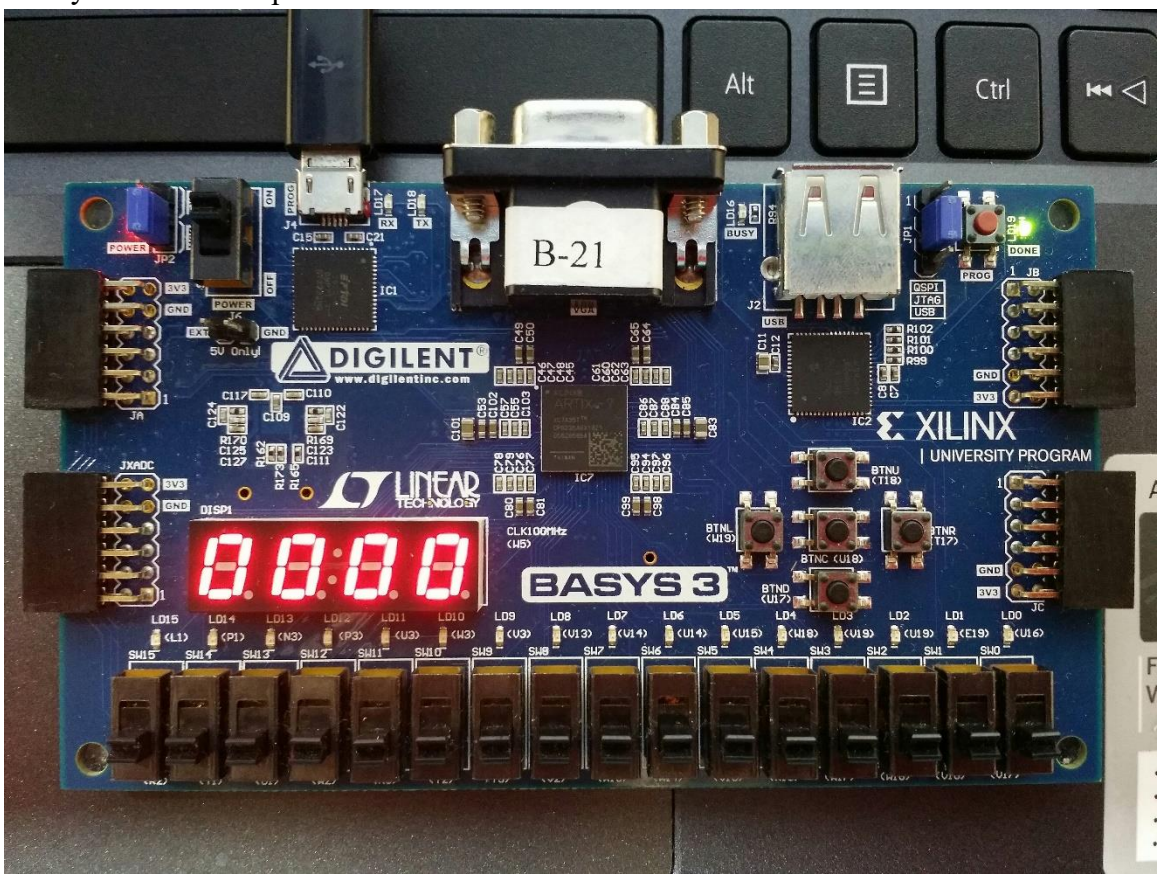
```
23  module binary_to_SSD_decoder_test();
24      // output
25      wire [7:0] D;   // 7-segment display decode
26      wire [3:0] d;   // LEDs to monitor
27
28      // input
29      reg  [3:0] i;   // 4-bit binary number
30
31      // instantiate
32      binary_to_SSD_decoder DUT(
33          .D(D),      // 7-segment display decode
34          .d(d),      // four LEDs to monitor the 4-bit binary number
35          .i(i)       // 4-bit binary number
36          );
37
38      // stimulus
39      initial
40          i = 0;
41      always
42          #10 i = i + 1;
43
44  endmodule           // binary_to_SSD_decoder_test
```

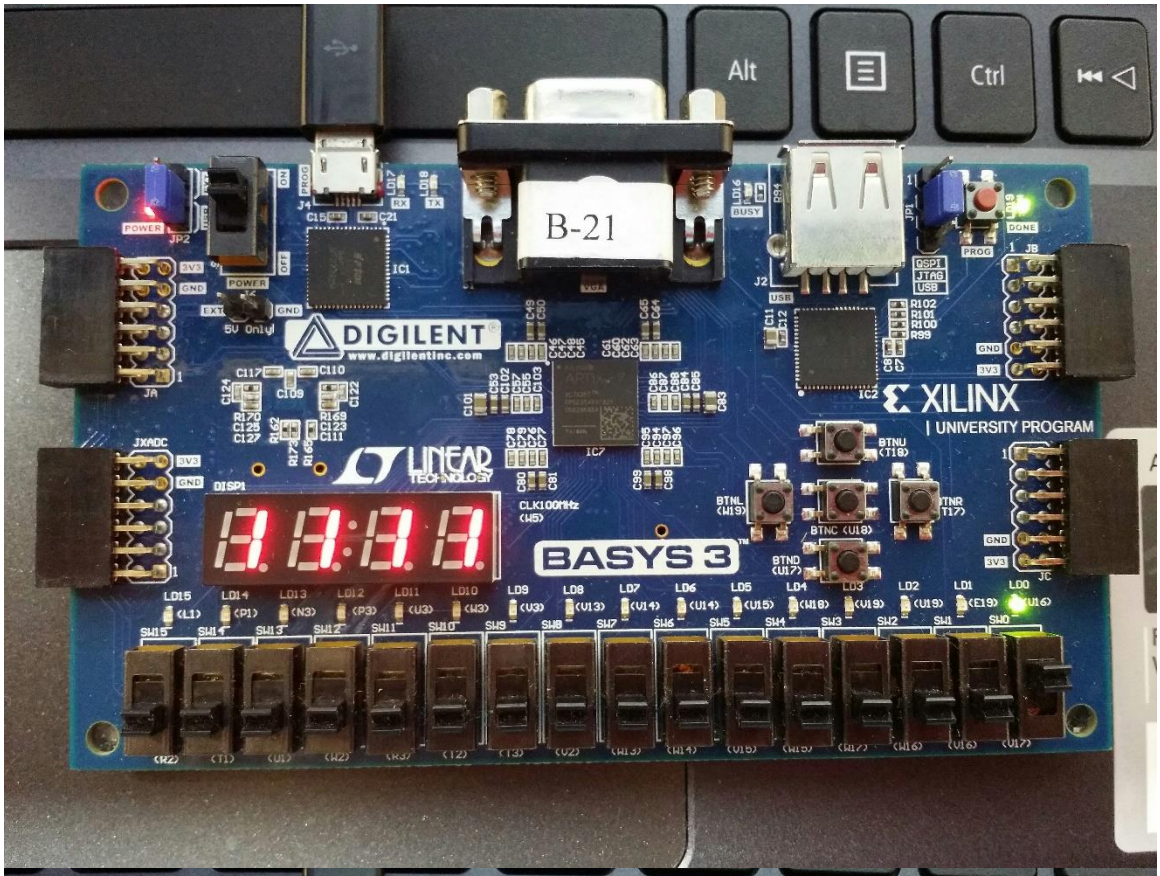


3.5 I/O Pins Assignment

Name	Direction	Package Pin	I/O Std
All ports (16)			
D (8)	OUT		LVCMOS33*
D[7]	OUT	W7	LVCMOS33*
D[6]	OUT	W6	LVCMOS33*
D[5]	OUT	U8	LVCMOS33*
D[4]	OUT	V8	LVCMOS33*
D[3]	OUT	U5	LVCMOS33*
D[2]	OUT	V5	LVCMOS33*
D[1]	OUT	U7	LVCMOS33*
D[0]	OUT	V7	LVCMOS33*
d (4)	OUT		LVCMOS33*
d[3]	OUT	V19	LVCMOS33*
d[2]	OUT	U19	LVCMOS33*
d[1]	OUT	E19	LVCMOS33*
d[0]	OUT	U16	LVCMOS33*
i (4)	IN		LVCMOS33*
i[3]	IN	W17	LVCMOS33*
i[2]	IN	W16	LVCMOS33*
i[1]	IN	V16	LVCMOS33*
i[0]	IN	V17	LVCMOS33*

3.6 Synthesis and Implementation:

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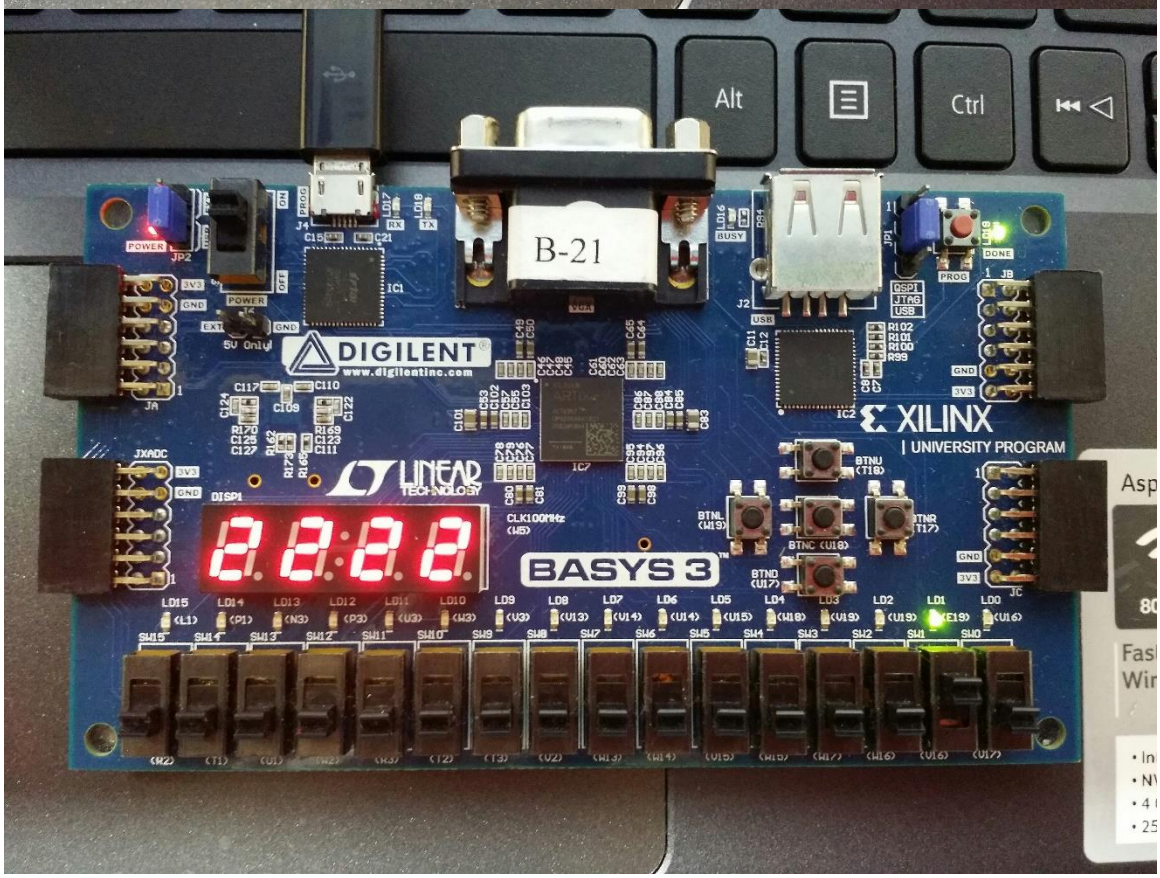
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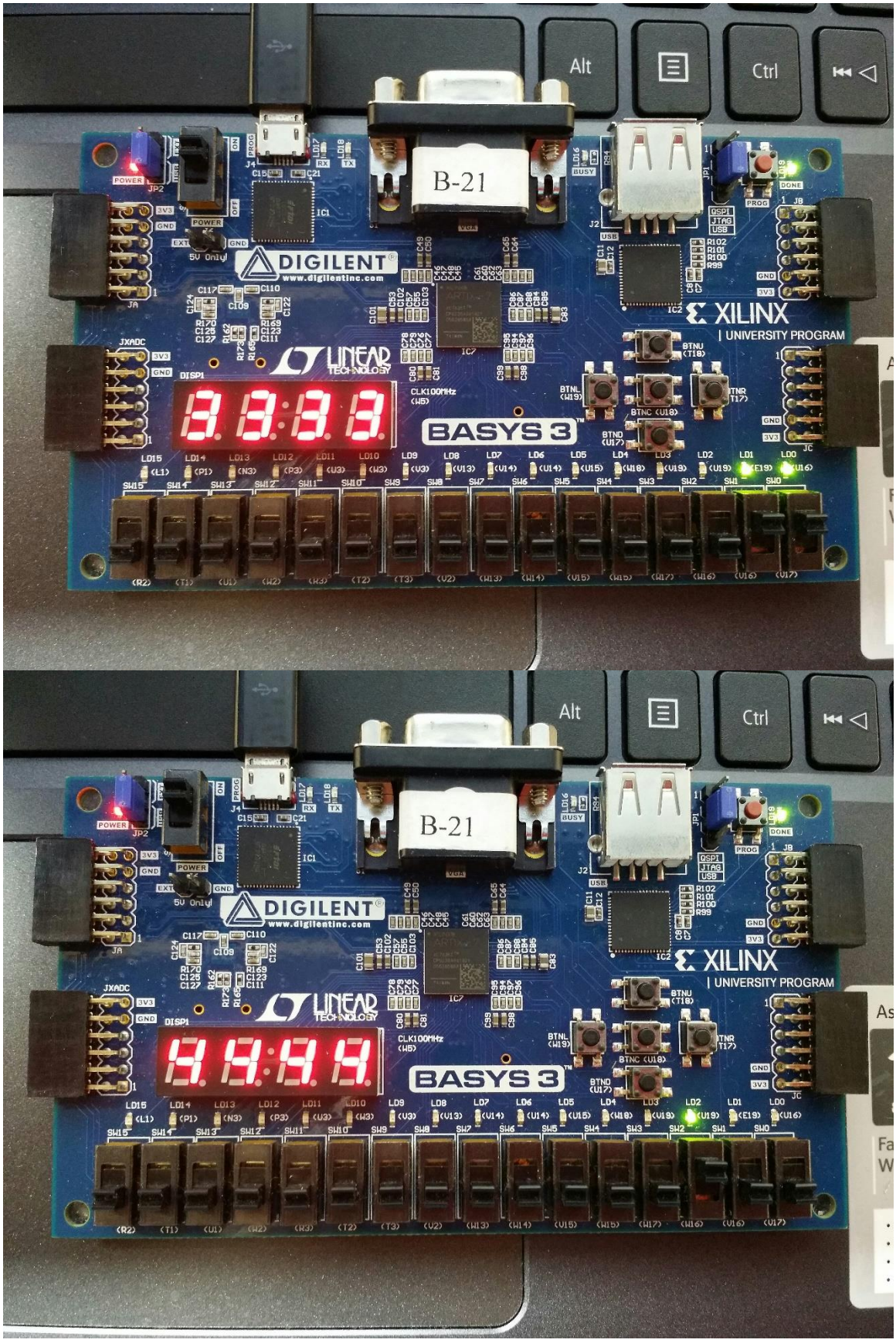
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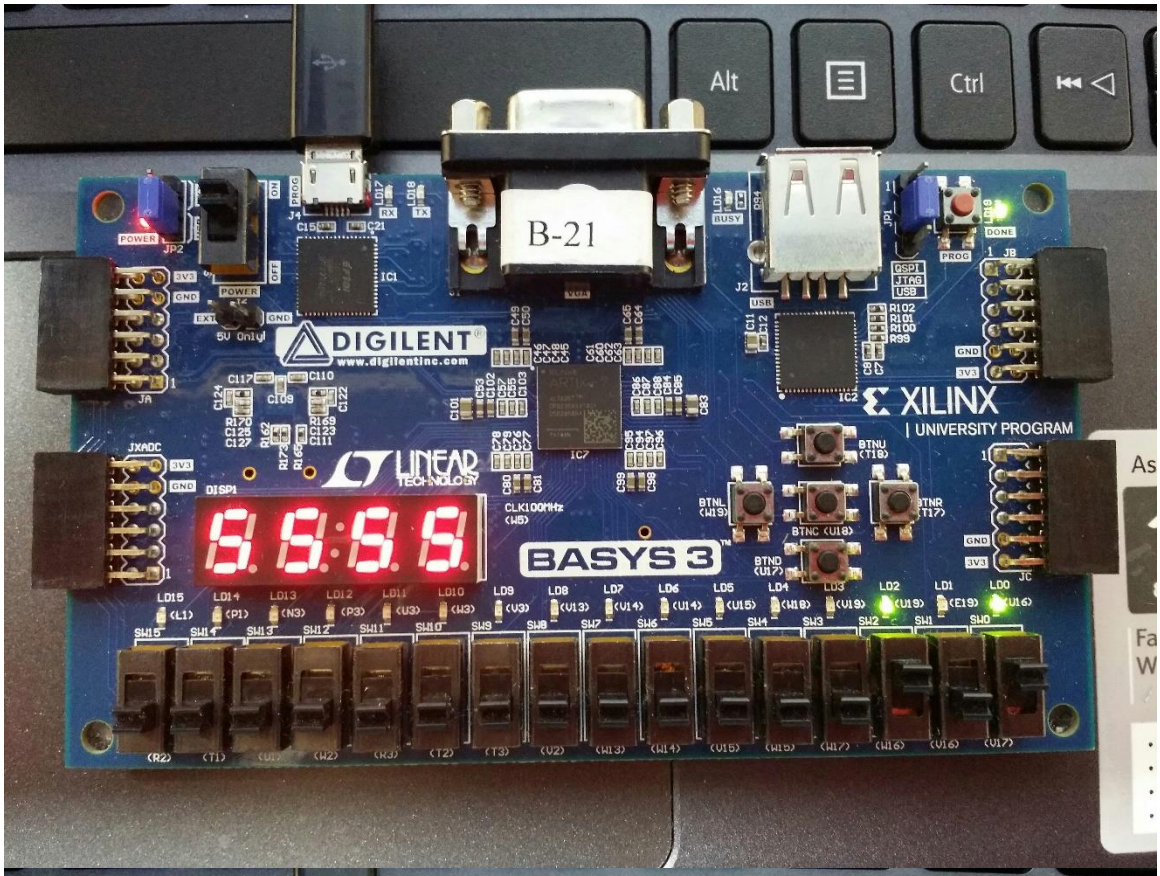
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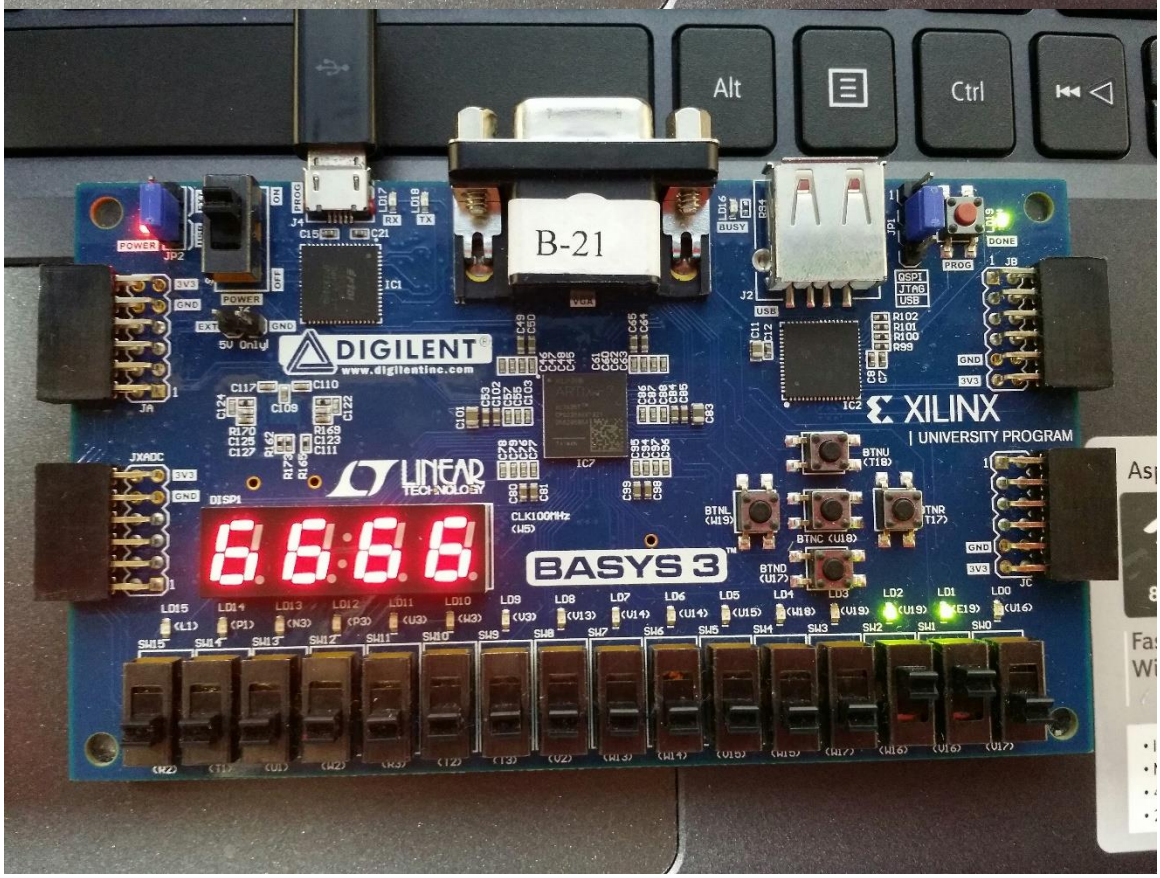
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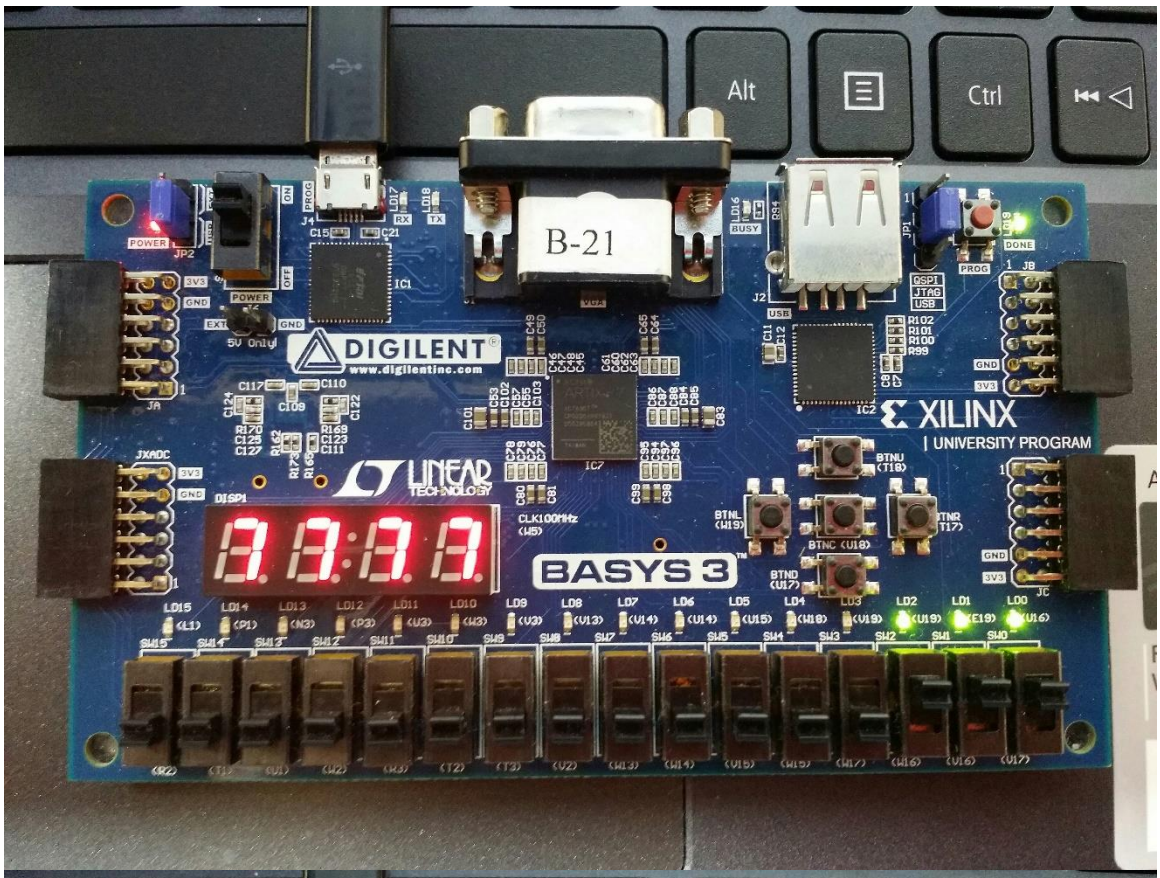
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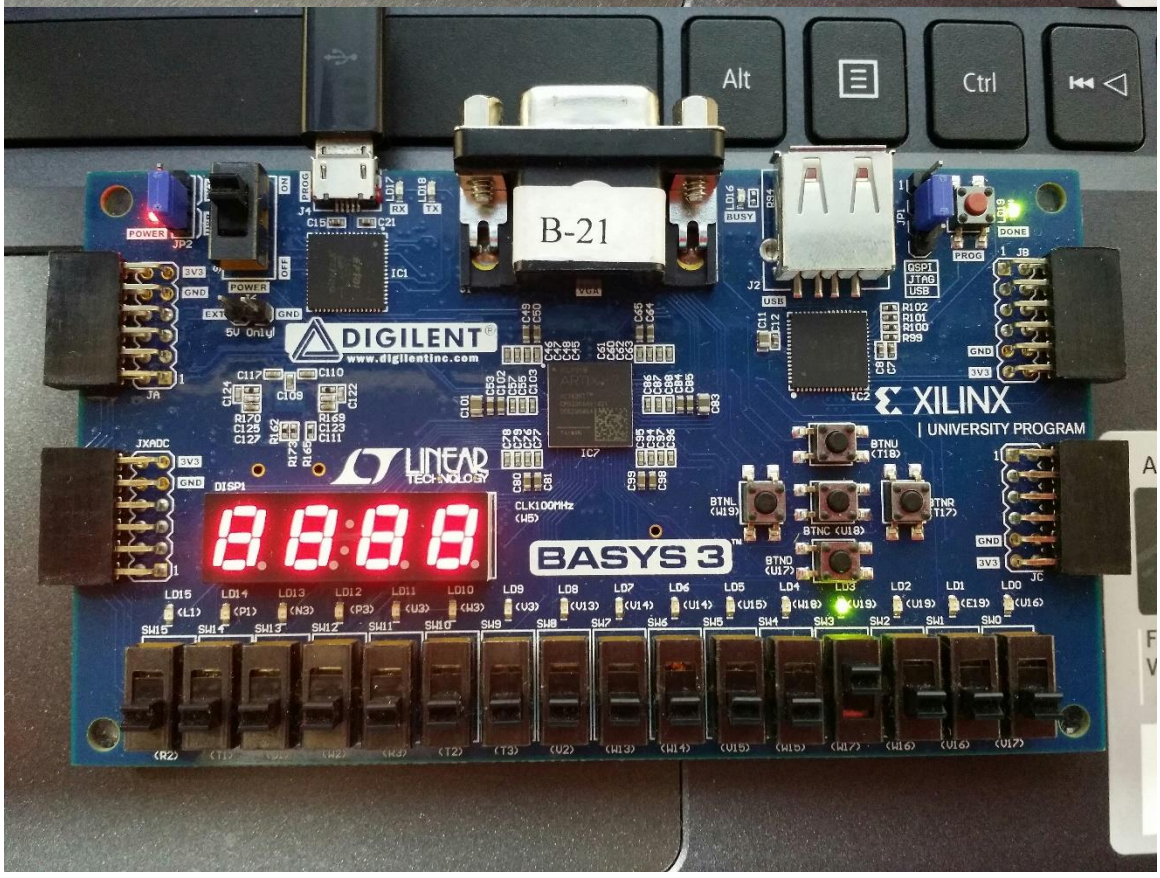
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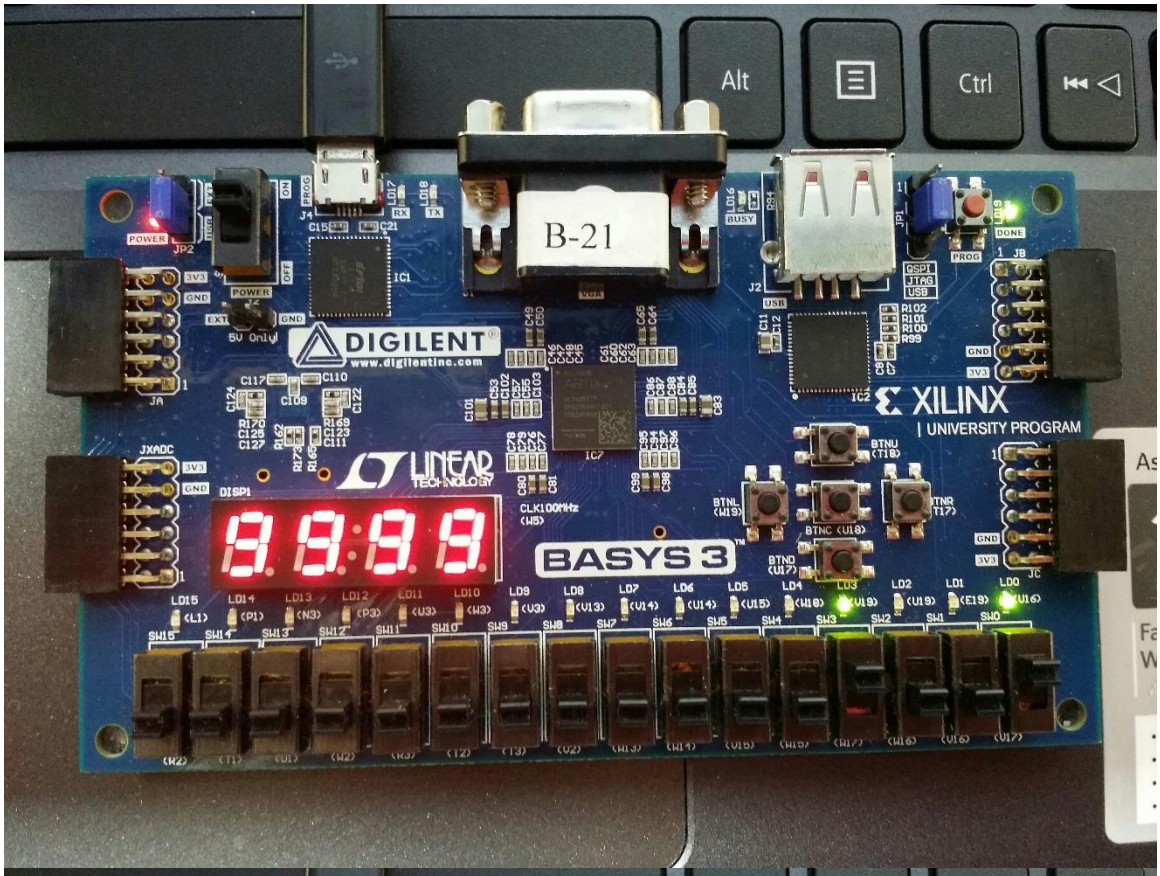
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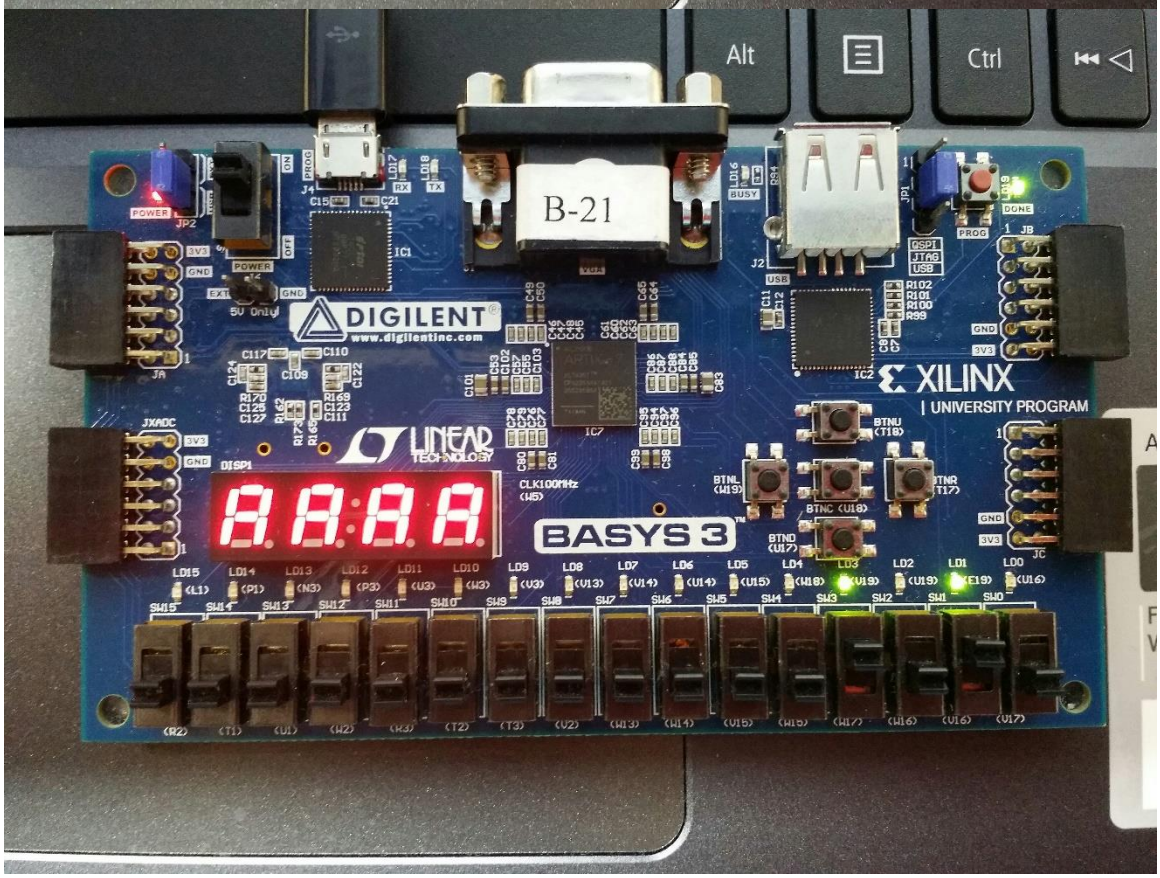
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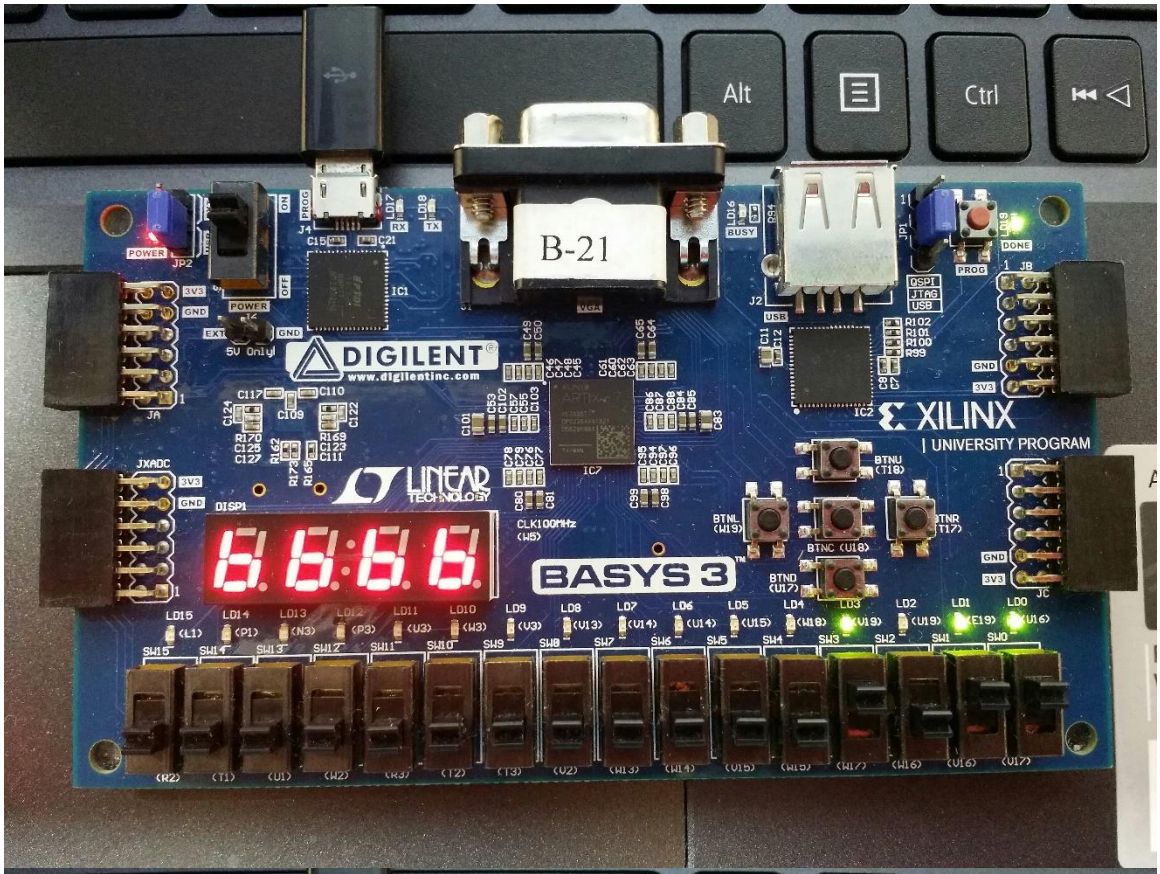
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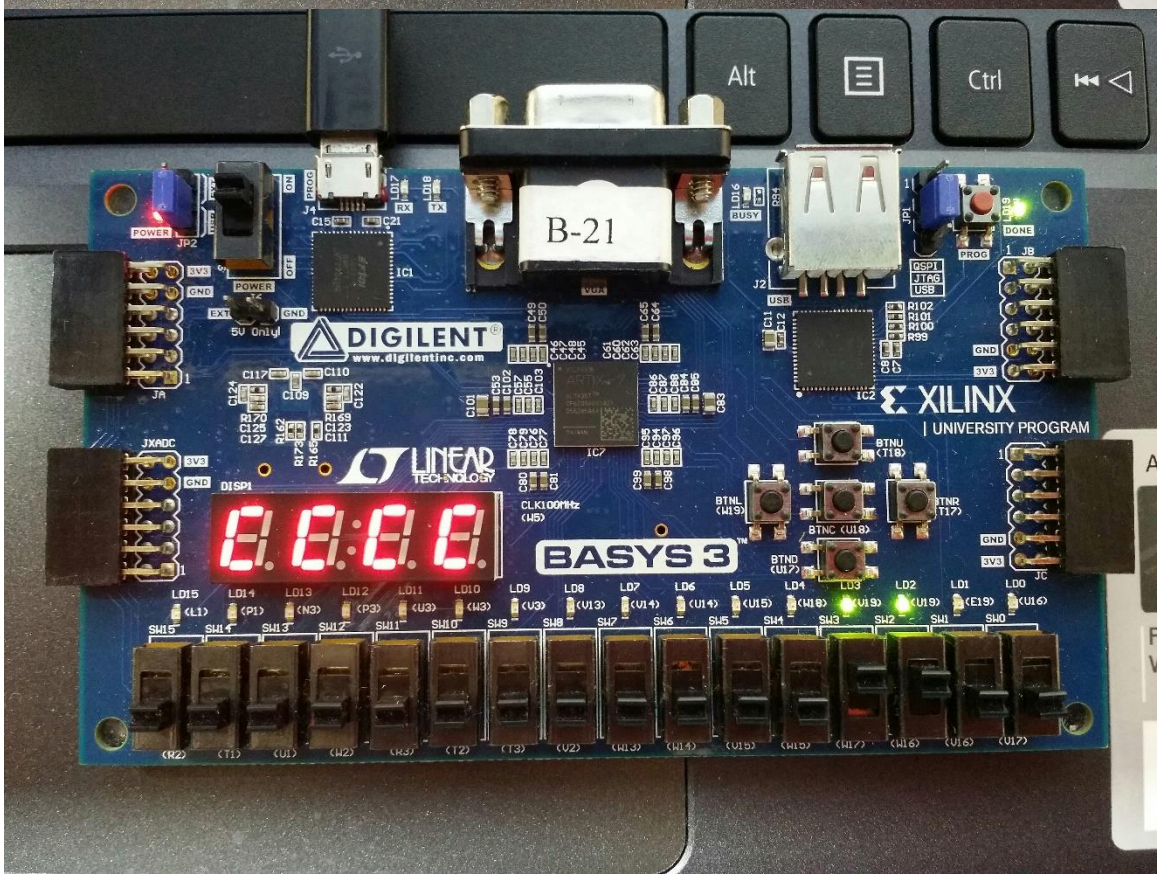
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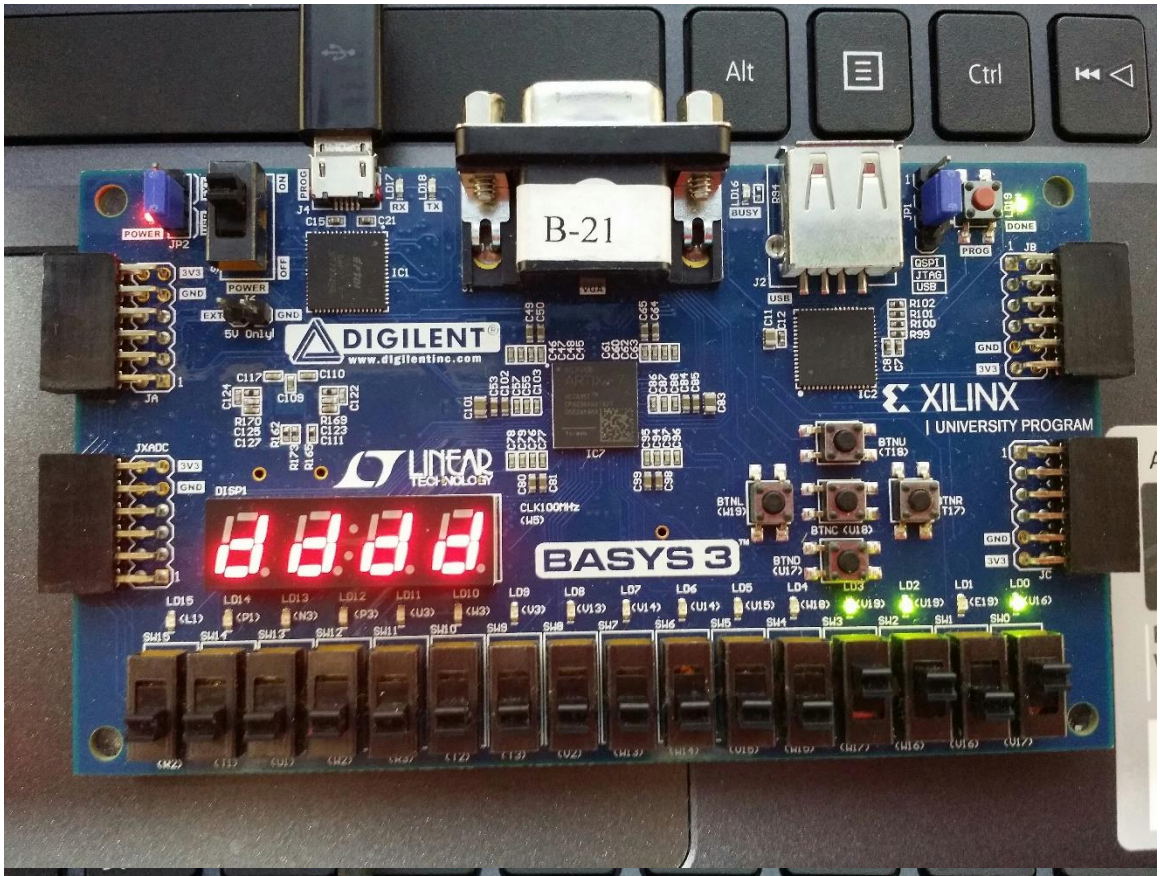
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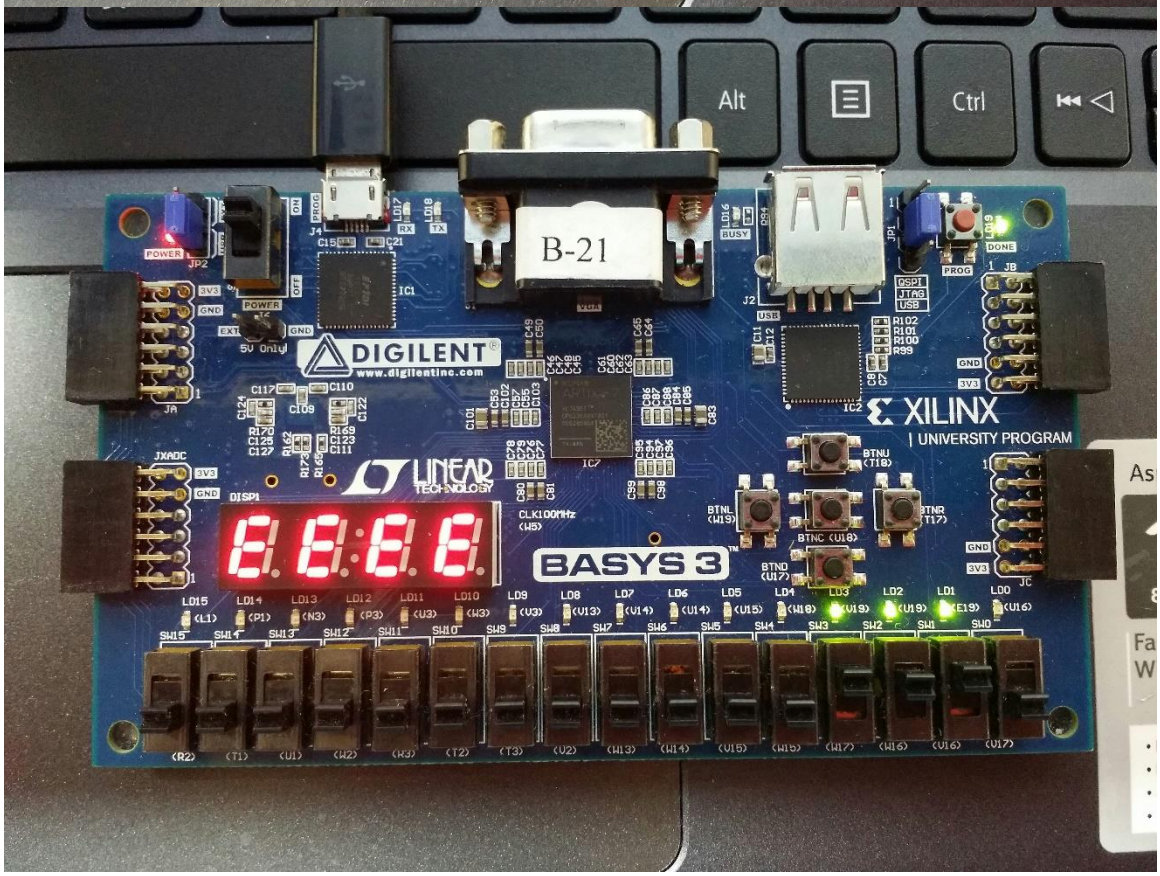
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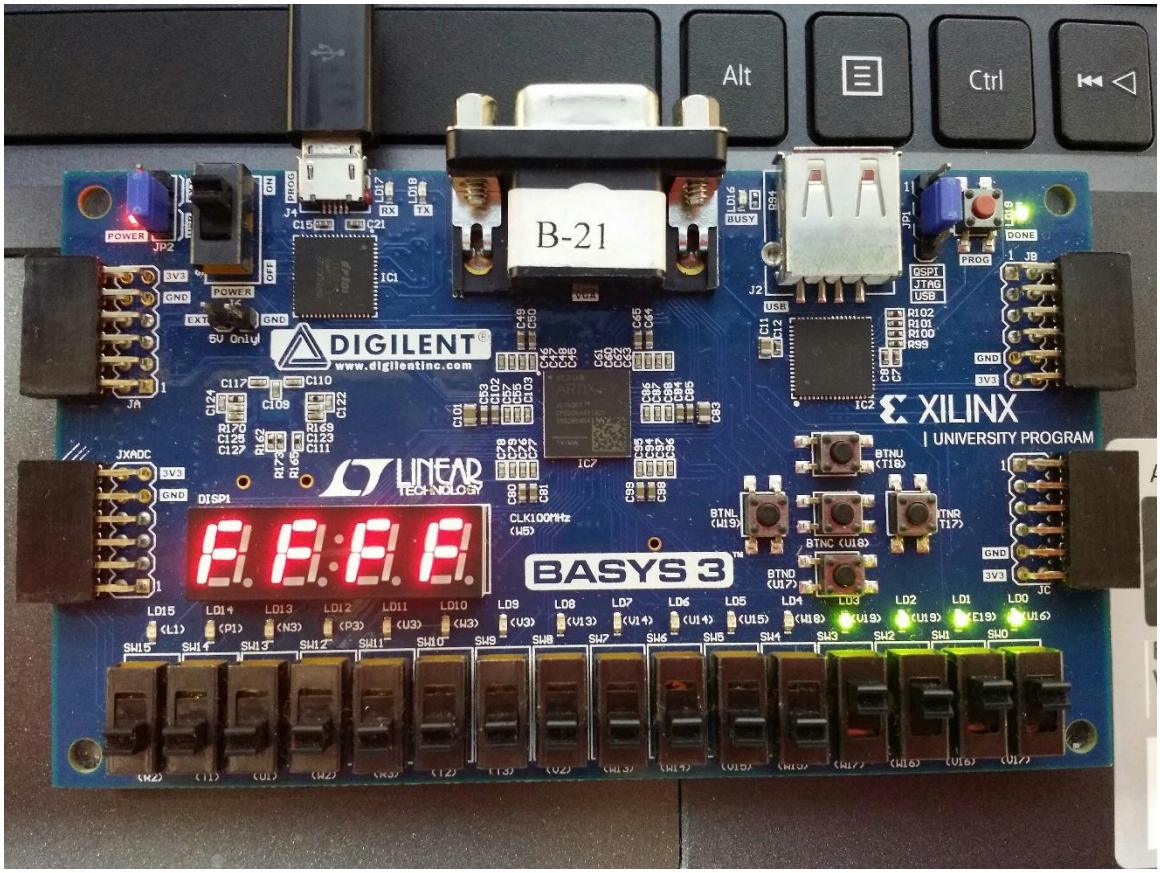
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SW15 SW14 SW13 SW12 SW11 SW10 SW9 SW8 SW7 SW6 SW5 SW4 SW3 SW2 SW1 SW0

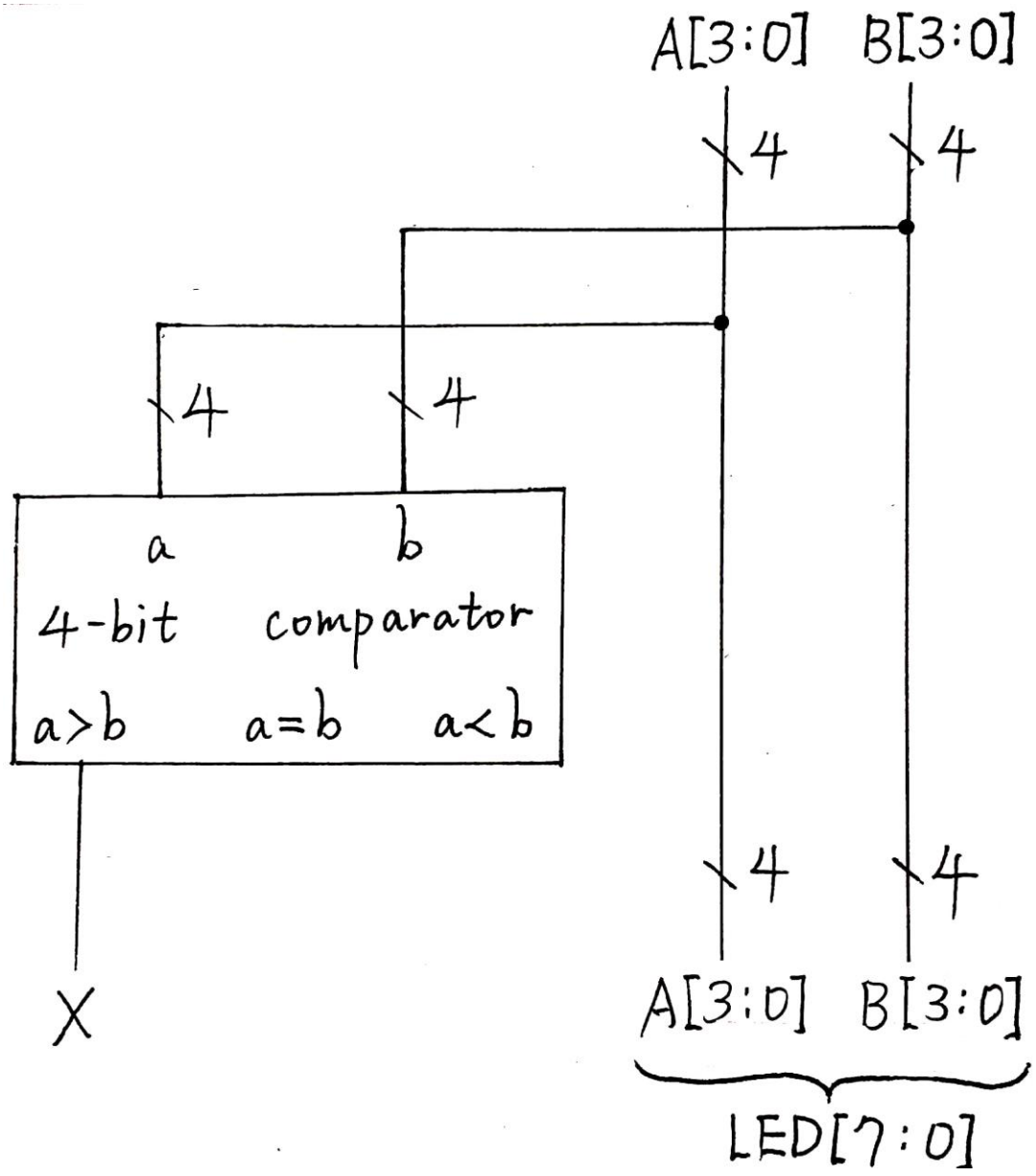
4. (Bonus) Design a combinational circuit that compares two 4-bit unsigned numbers A andB to see whether A is greater than B. The circuit has one output X such that X = 0 if A ≤ B and X = 1 if A > B. (let A[3:0], B[3:0] be controlled by 8 DIP switches, the binary numbers are displayed on 8 LEDs. The result X is on another LED.)

4.1 I/O:

inputs: A[3:0],
B[3:0],

outputs: X
LED[7:0]

4.2 Circuit Diagram:

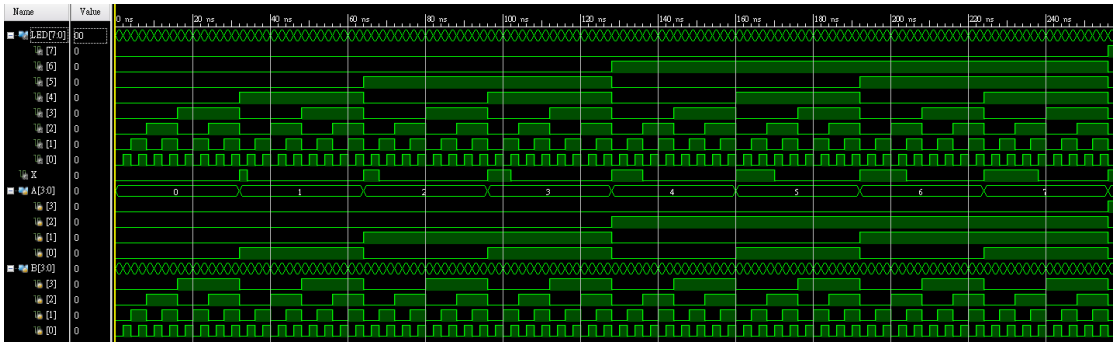


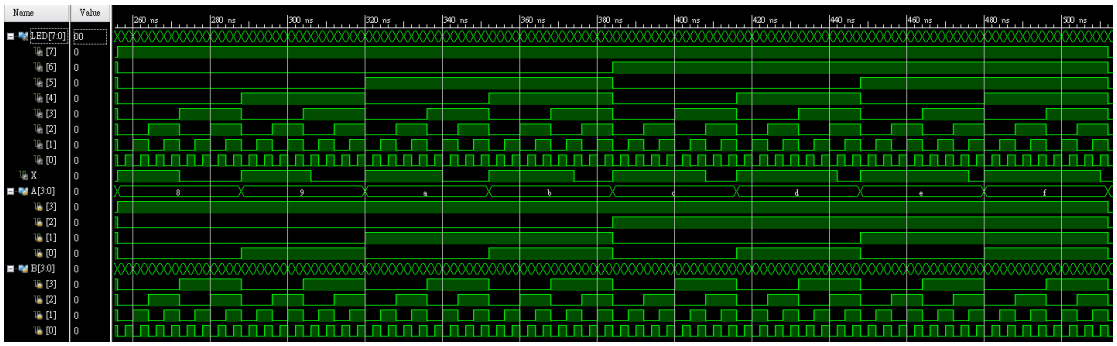
4.3 Verilog HDL Coding:

```
23 module comparator(
24     output [7:0] LED,  // 8 LEDs displaying A and B
25     output       X,    // X = 0 if A ? B and X = 1 if A > B
26     input  [3:0] A,    // 4-bit unsigned number to compare
27     input  [3:0] B     // 4-bit unsigned number to compare
28     );
29
30     assign LED = {A, B};  // 8 LEDs displaying A and B
31     assign X = (A > B);   // X = 0 if A ? B and X = 1 if A > B
32
33 endmodule               // comparator
```

4.4 Testbench Verification:

```
23 module comparator_test();
24     // output
25     wire [7:0] LED;  // 8 LEDs displaying A and B
26     wire       X;    // X = 0 if A ? B and X = 1 if A > B
27
28     // input
29     reg  [3:0] A;    // 4-bit unsigned number to compare
30     reg  [3:0] B;    // 4-bit unsigned number to compare
31
32     // instantiate
33     comparator DUT(
34         .LED(LED),  // 8 LEDs displaying A and B
35         .X(X),      // X = 0 if A ? B and X = 1 if A > B
36         .A(A),      // 4-bit unsigned number to compare
37         .B(B)       // 4-bit unsigned number to compare
38         );
39
40     // stimulus
41     initial
42         {A, B} = 0;
43     always
44         #2 {A, B} = {A, B} + 1;
45
46 endmodule
```

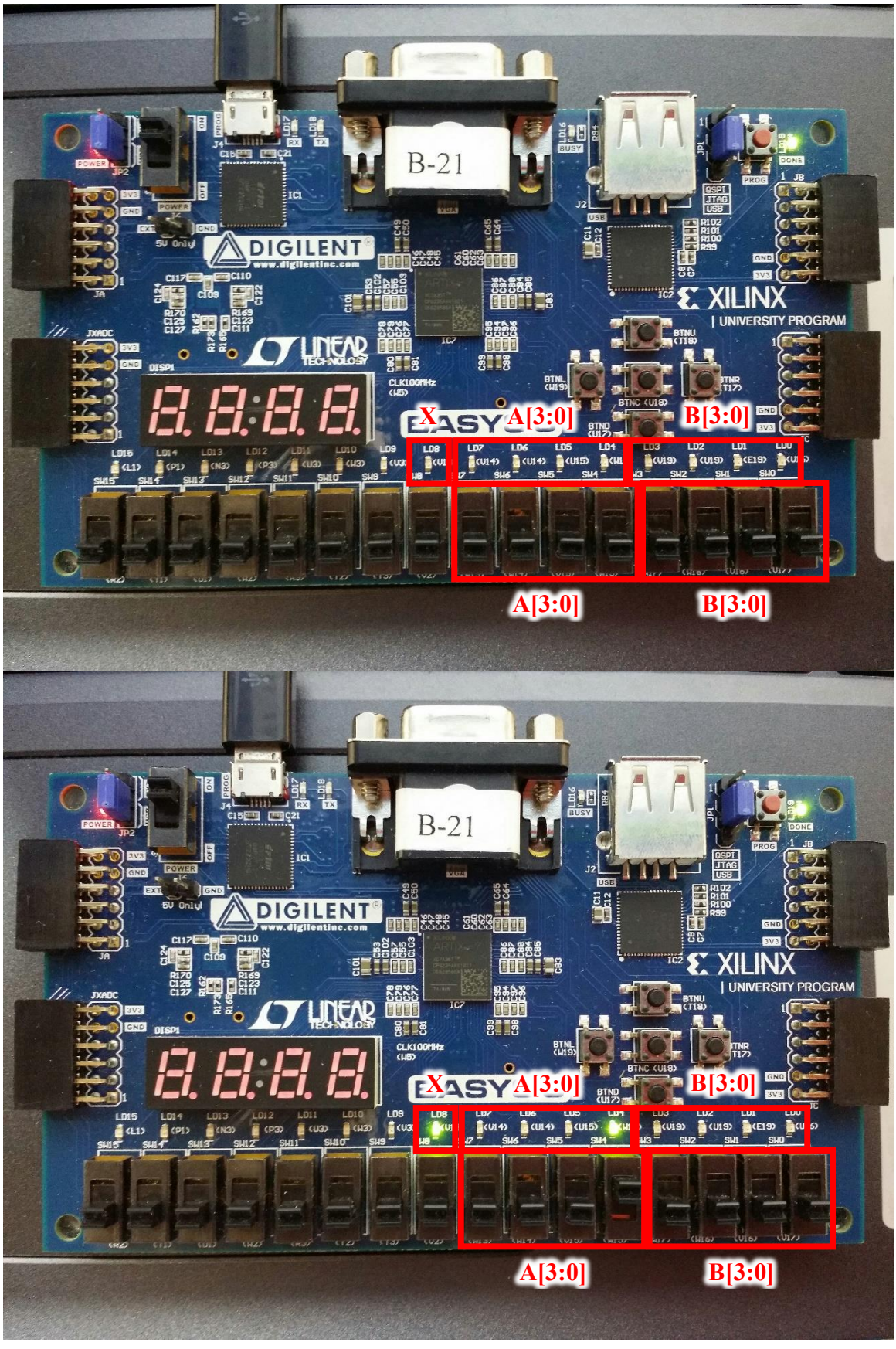


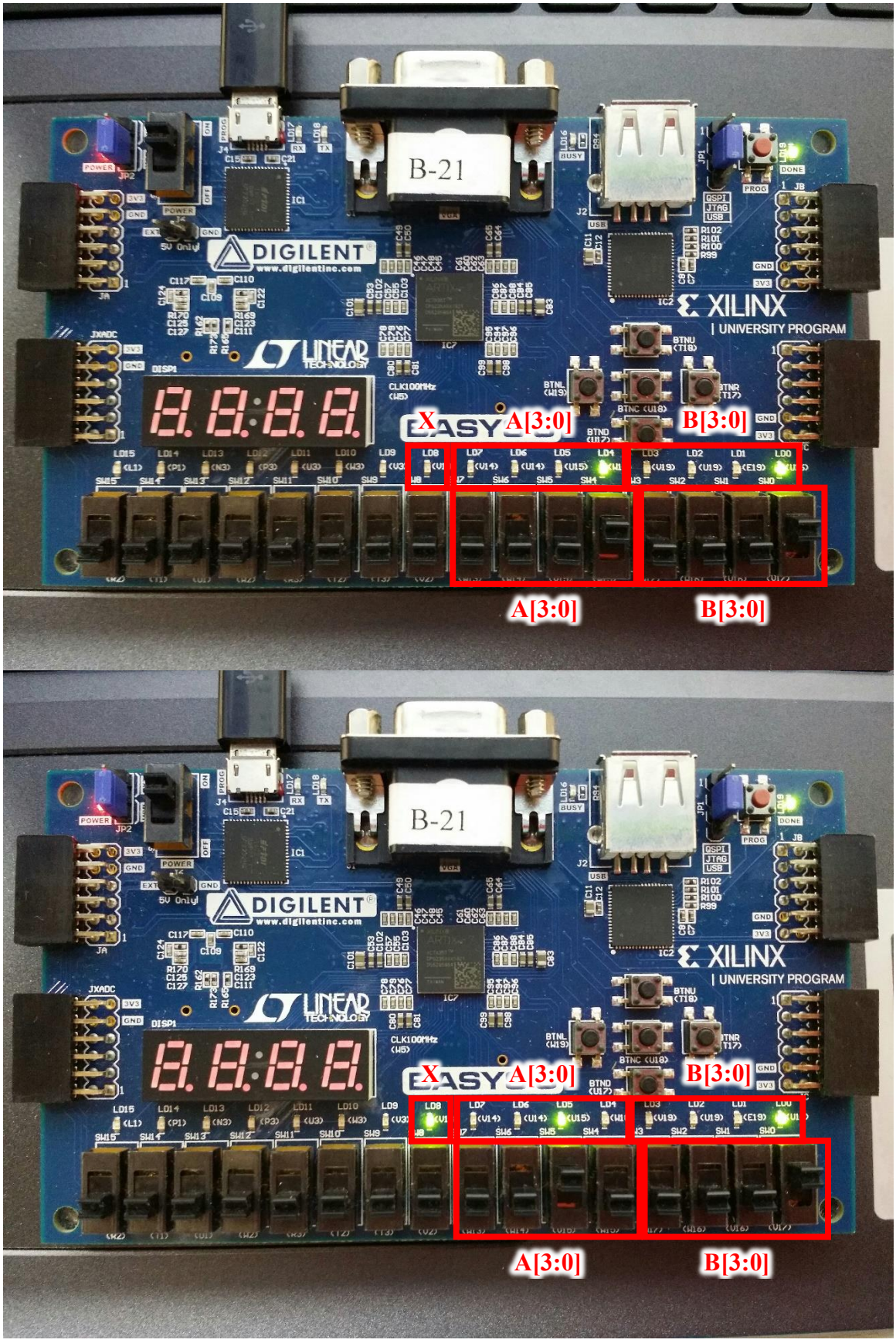


4.5 I/O Pins Assignment

Name	Direction	Package Pin	I/O Std
All ports (17)			
A (4)	IN		LVCMOS33*
A[3]	IN	W13	LVCMOS33*
A[2]	IN	W14	LVCMOS33*
A[1]	IN	V15	LVCMOS33*
A[0]	IN	W15	LVCMOS33*
B (4)	IN		LVCMOS33*
B[3]	IN	W17	LVCMOS33*
B[2]	IN	W16	LVCMOS33*
B[1]	IN	V16	LVCMOS33*
B[0]	IN	V17	LVCMOS33*
LED (8)	OUT		LVCMOS33*
LED[7]	OUT	V14	LVCMOS33*
LED[6]	OUT	U14	LVCMOS33*
LED[5]	OUT	U15	LVCMOS33*
LED[4]	OUT	W18	LVCMOS33*
LED[3]	OUT	V19	LVCMOS33*
LED[2]	OUT	U19	LVCMOS33*
LED[1]	OUT	E19	LVCMOS33*
LED[0]	OUT	U16	LVCMOS33*
Scalar ports (1)			
X	OUT	V13	LVCMOS33*

4.6 Synthesis and Implementation:

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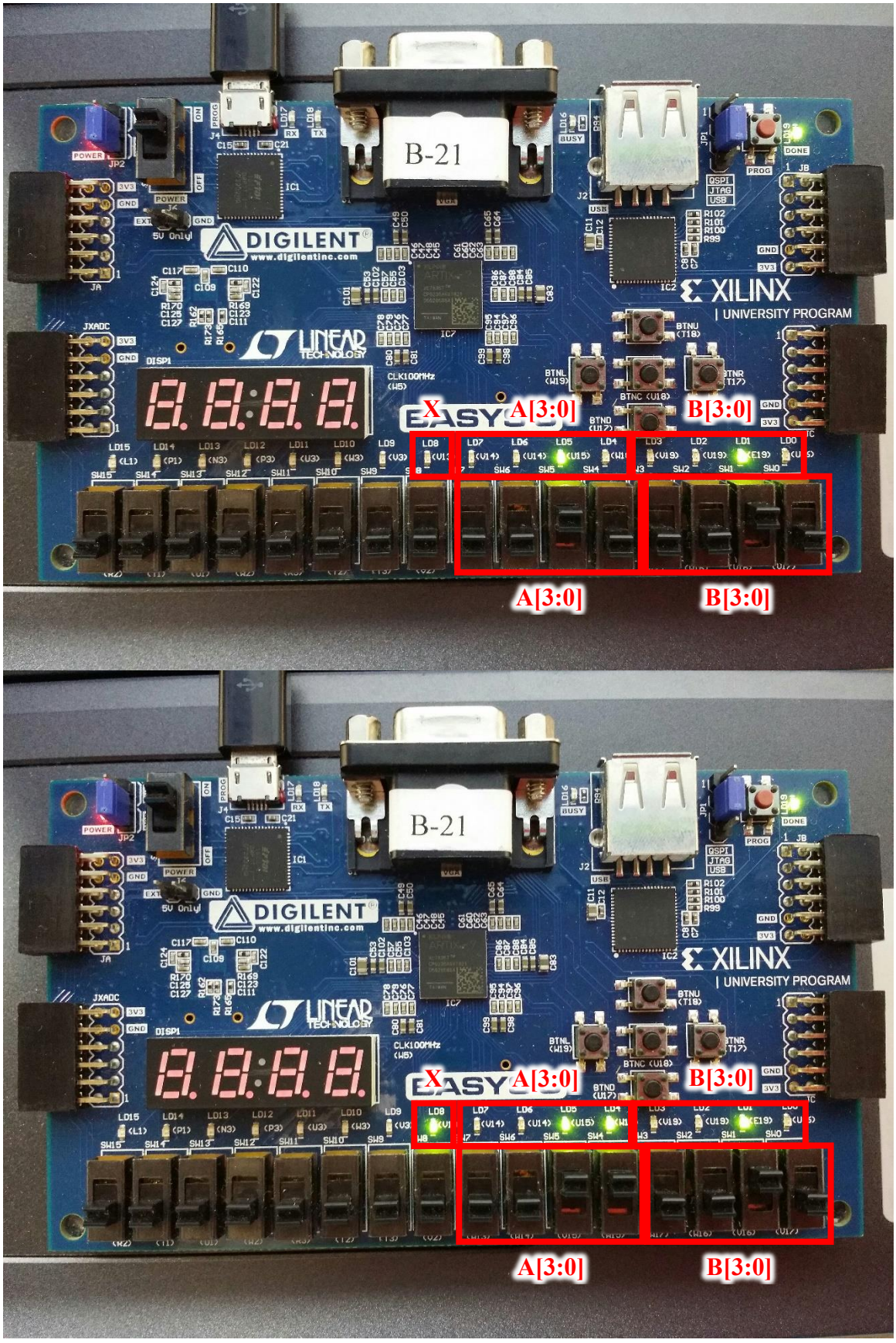
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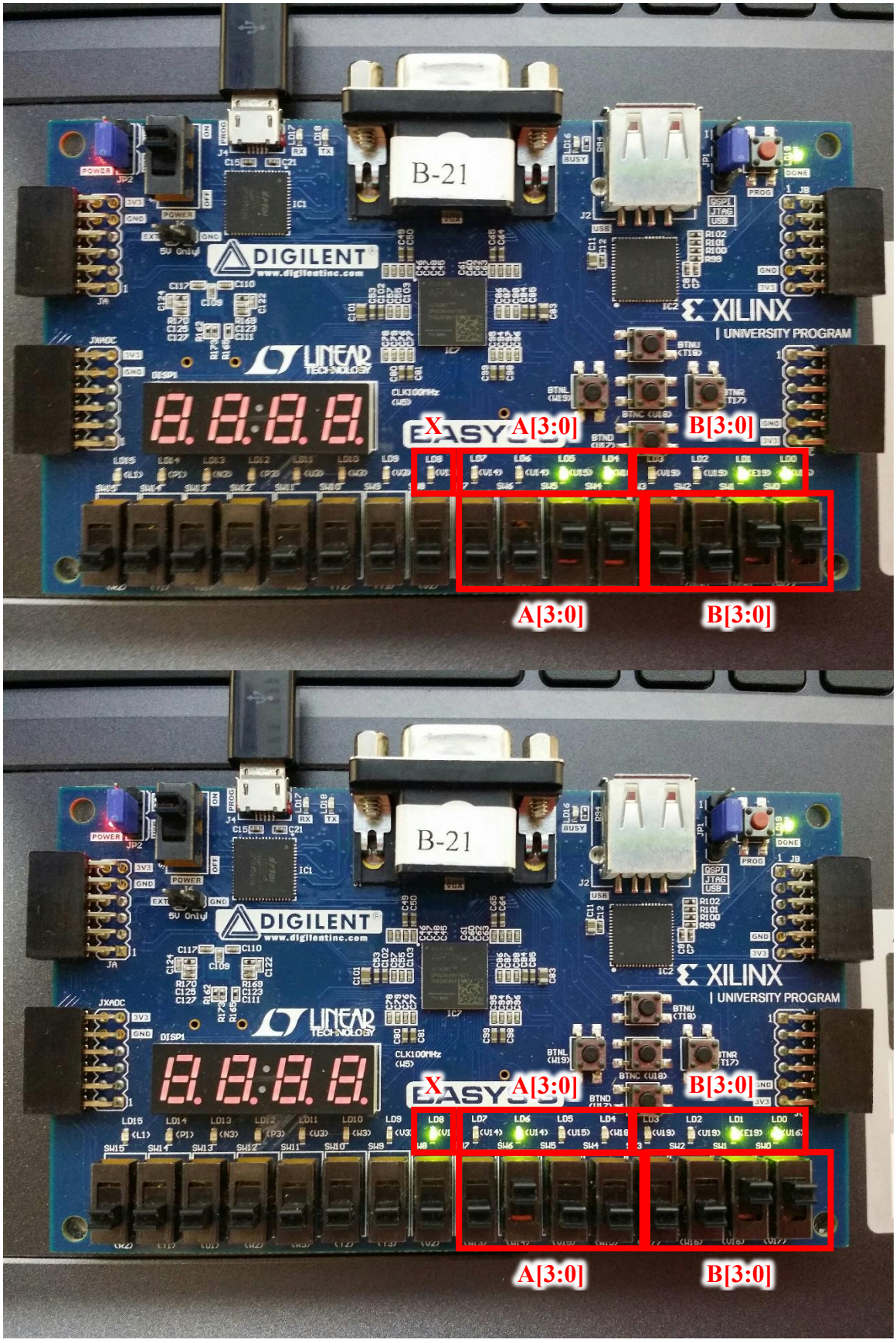
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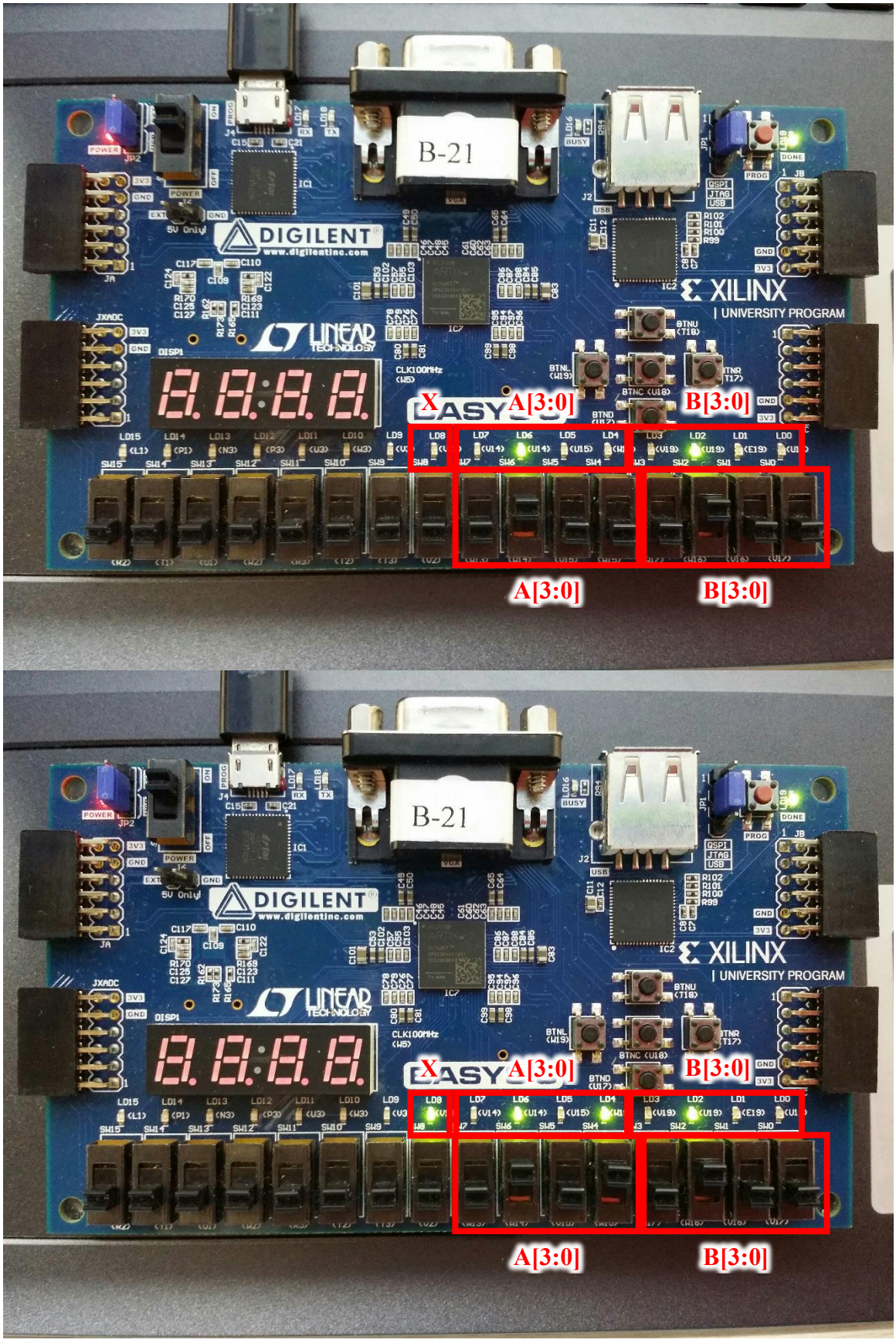
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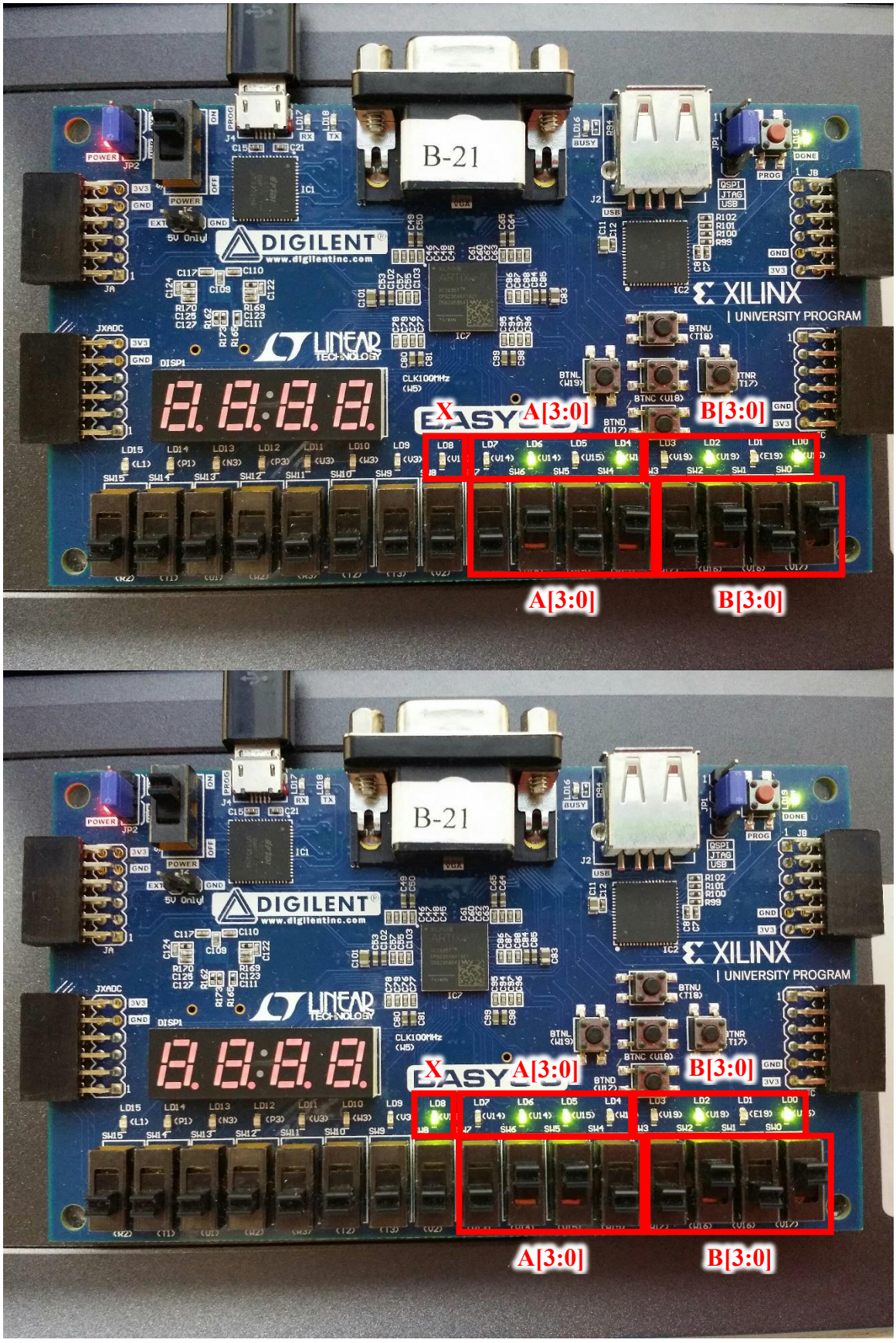
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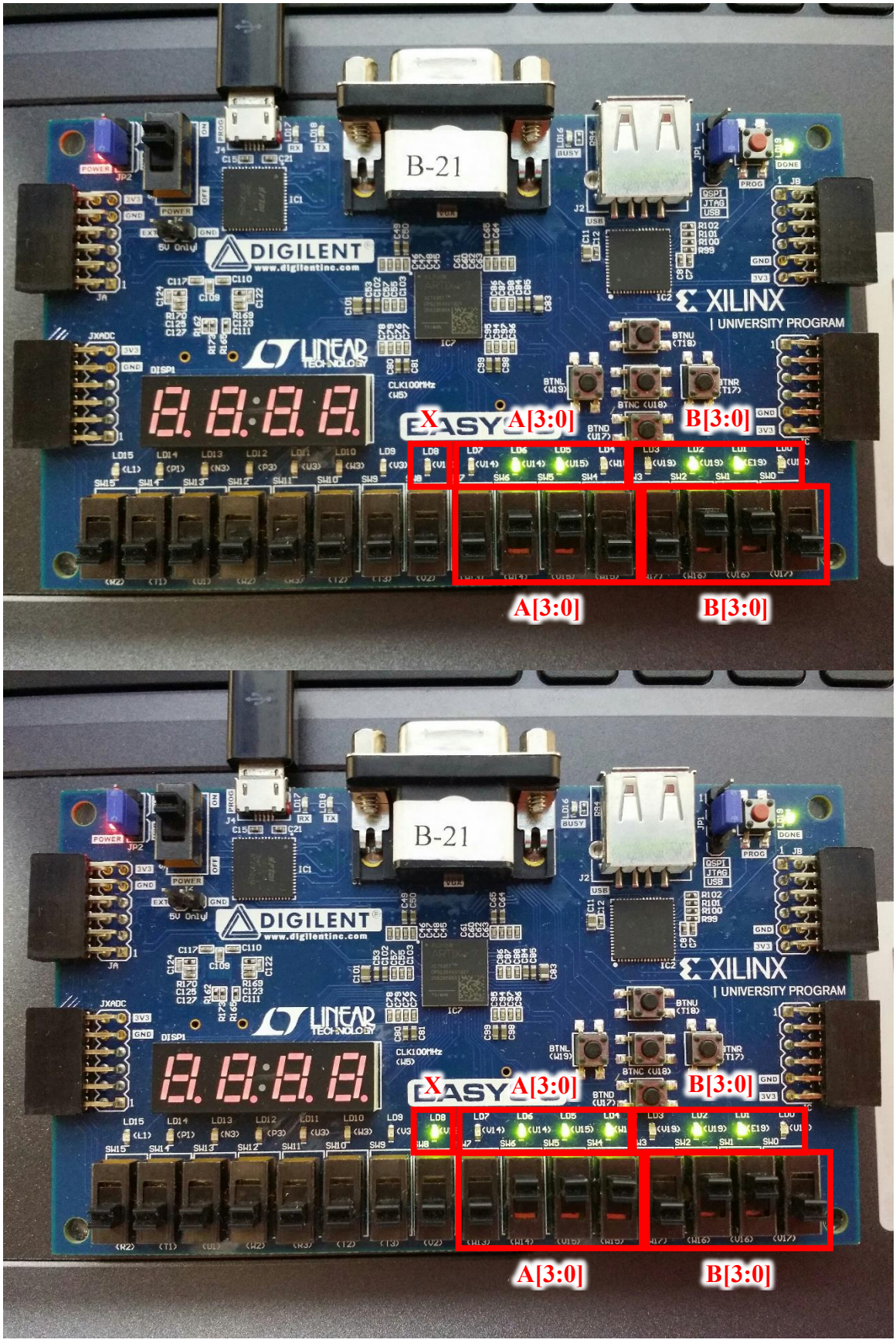
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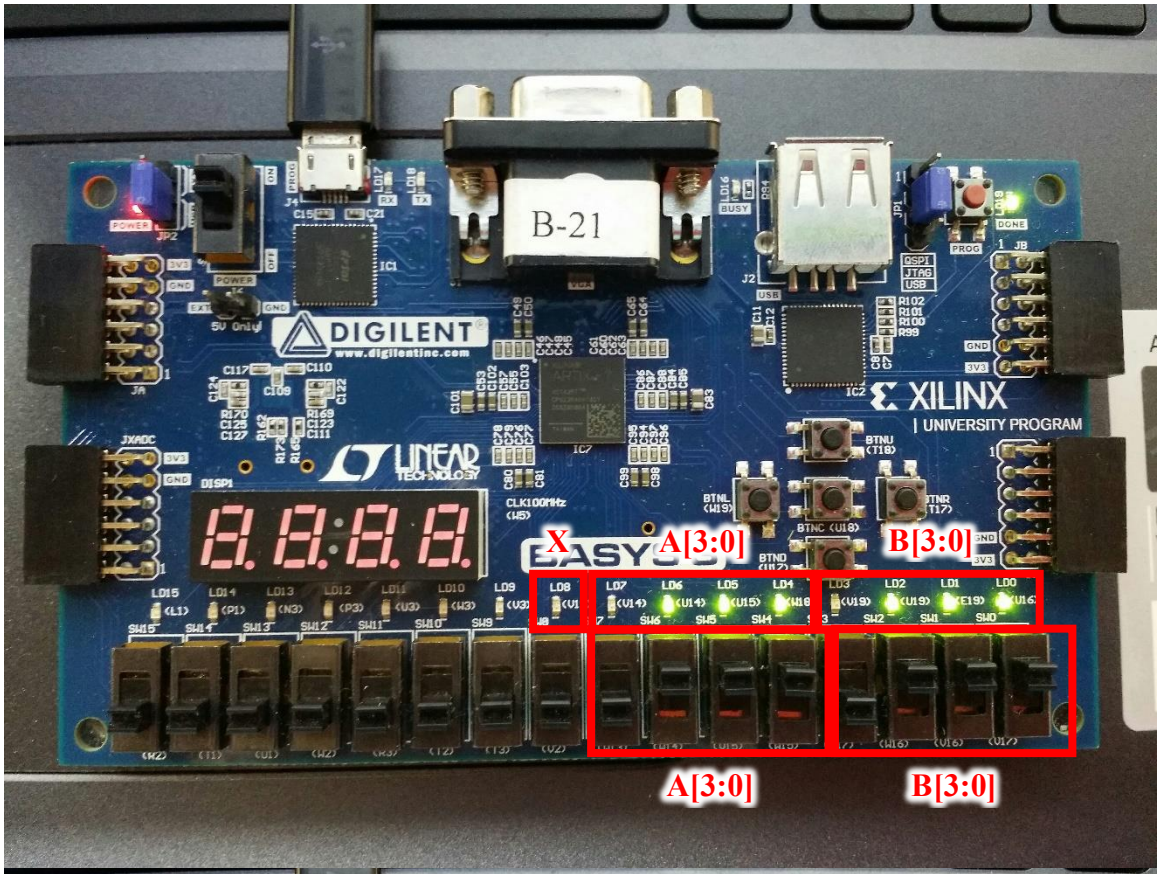
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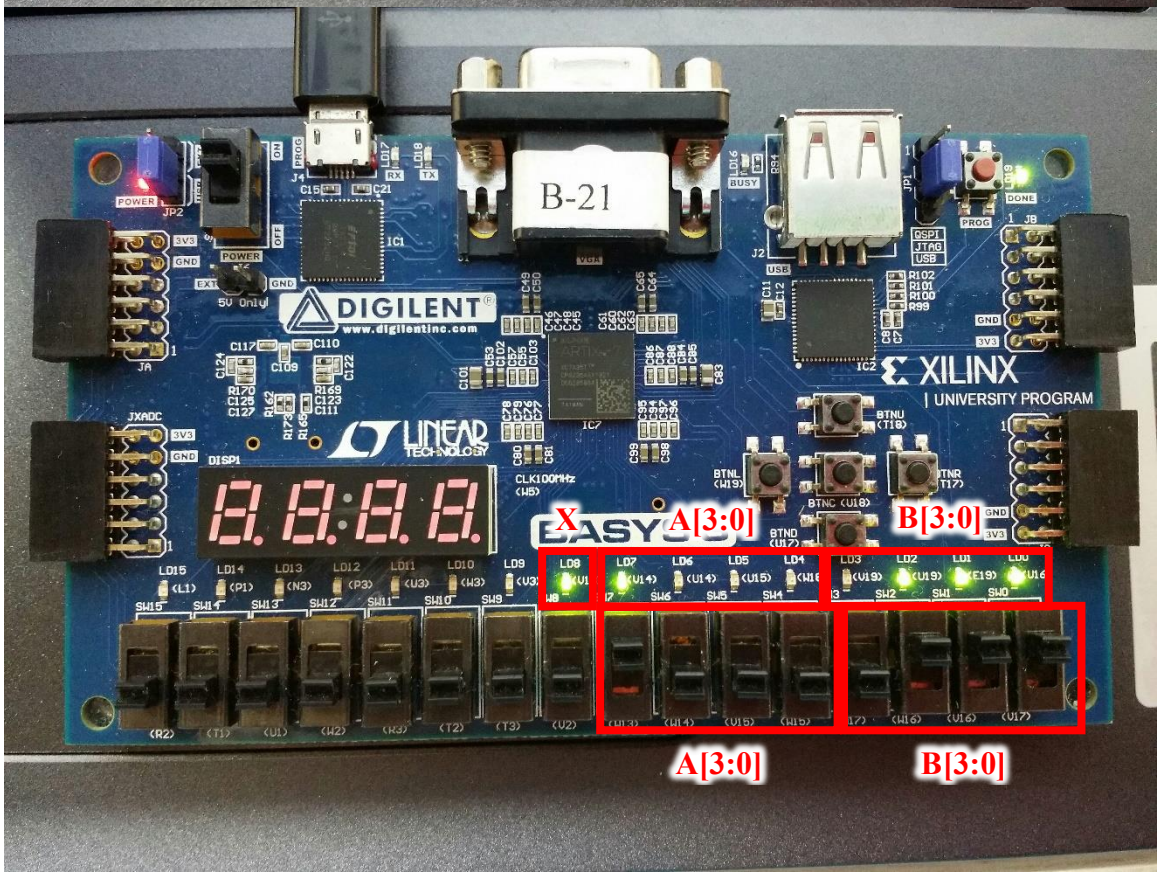
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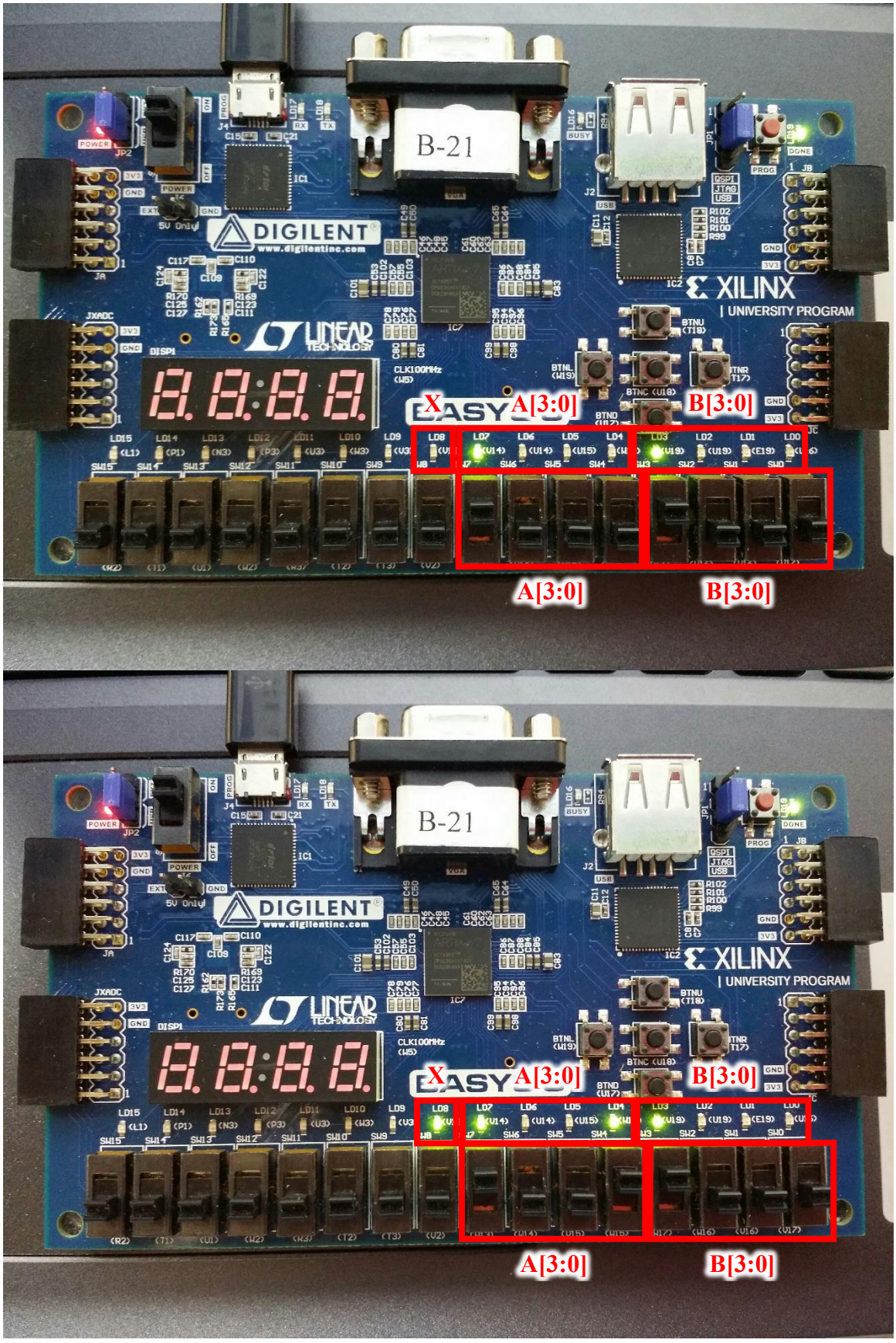
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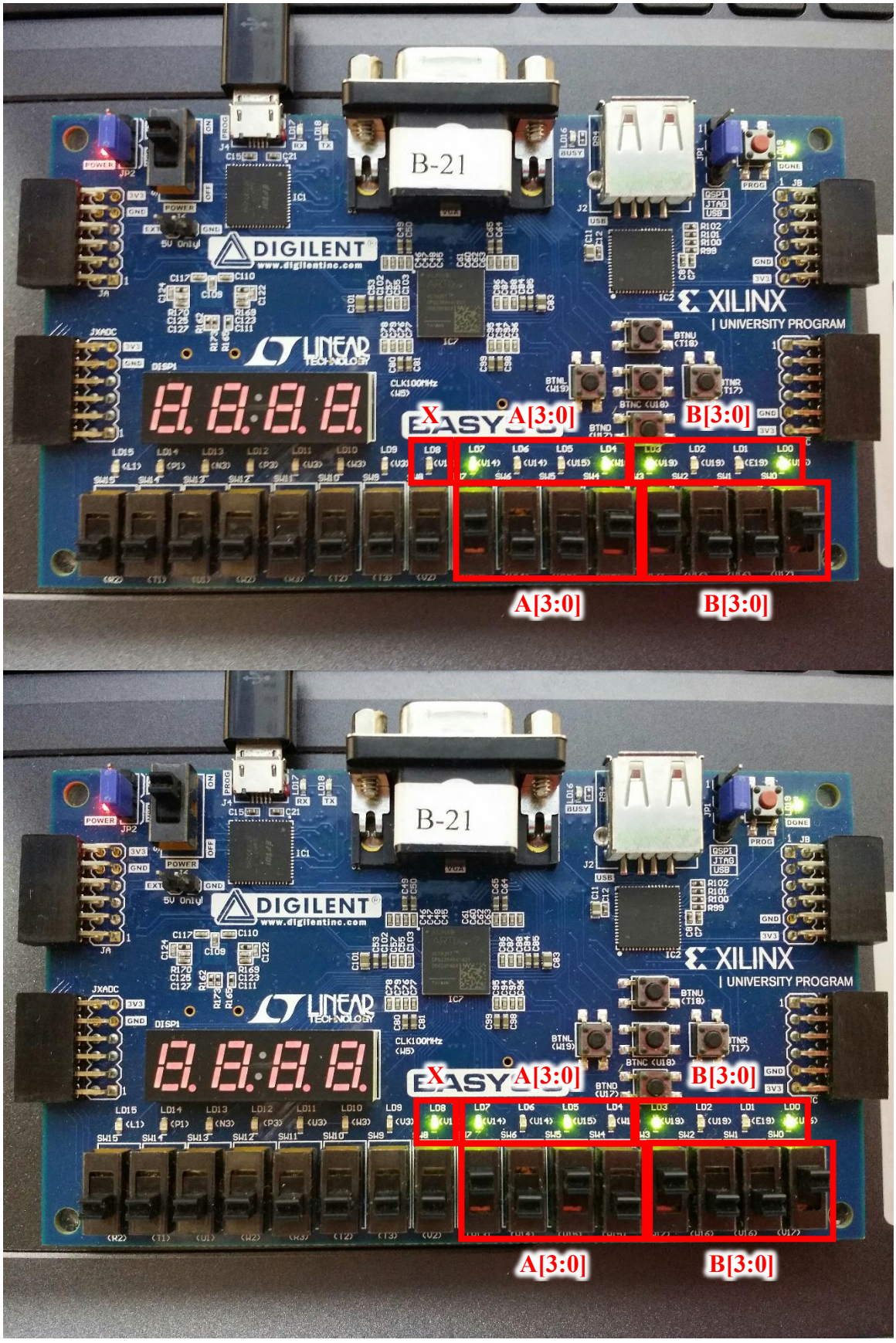
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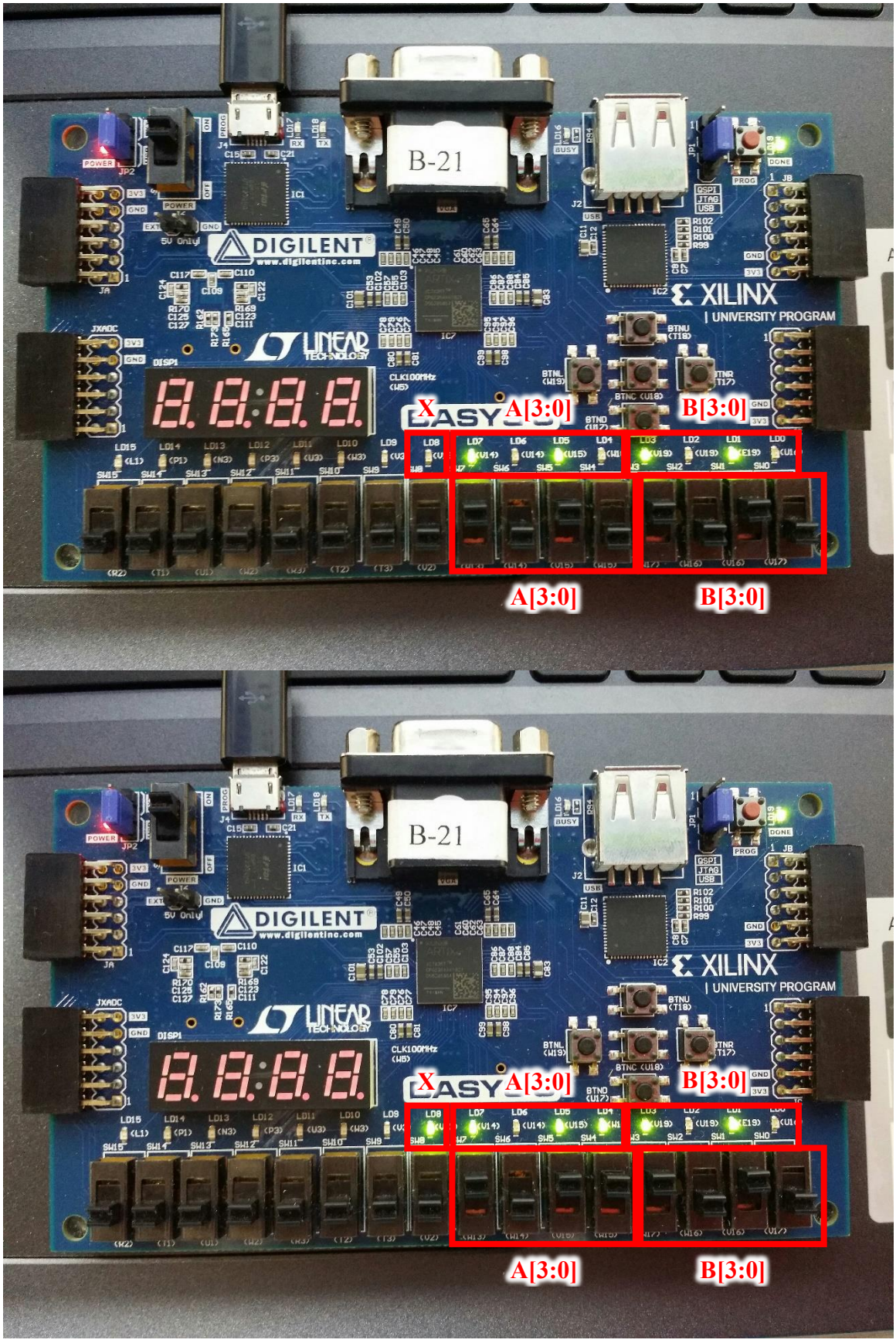
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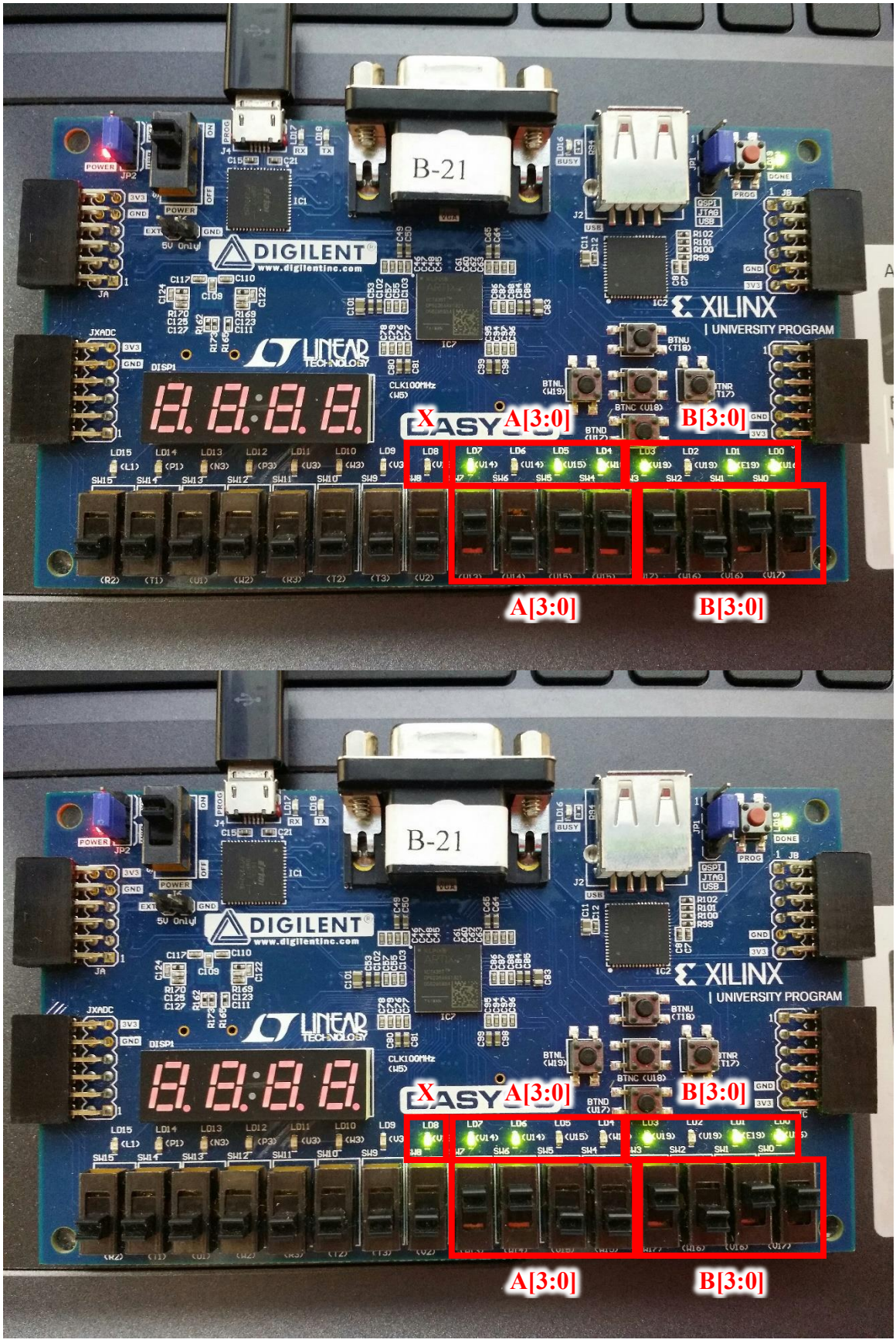
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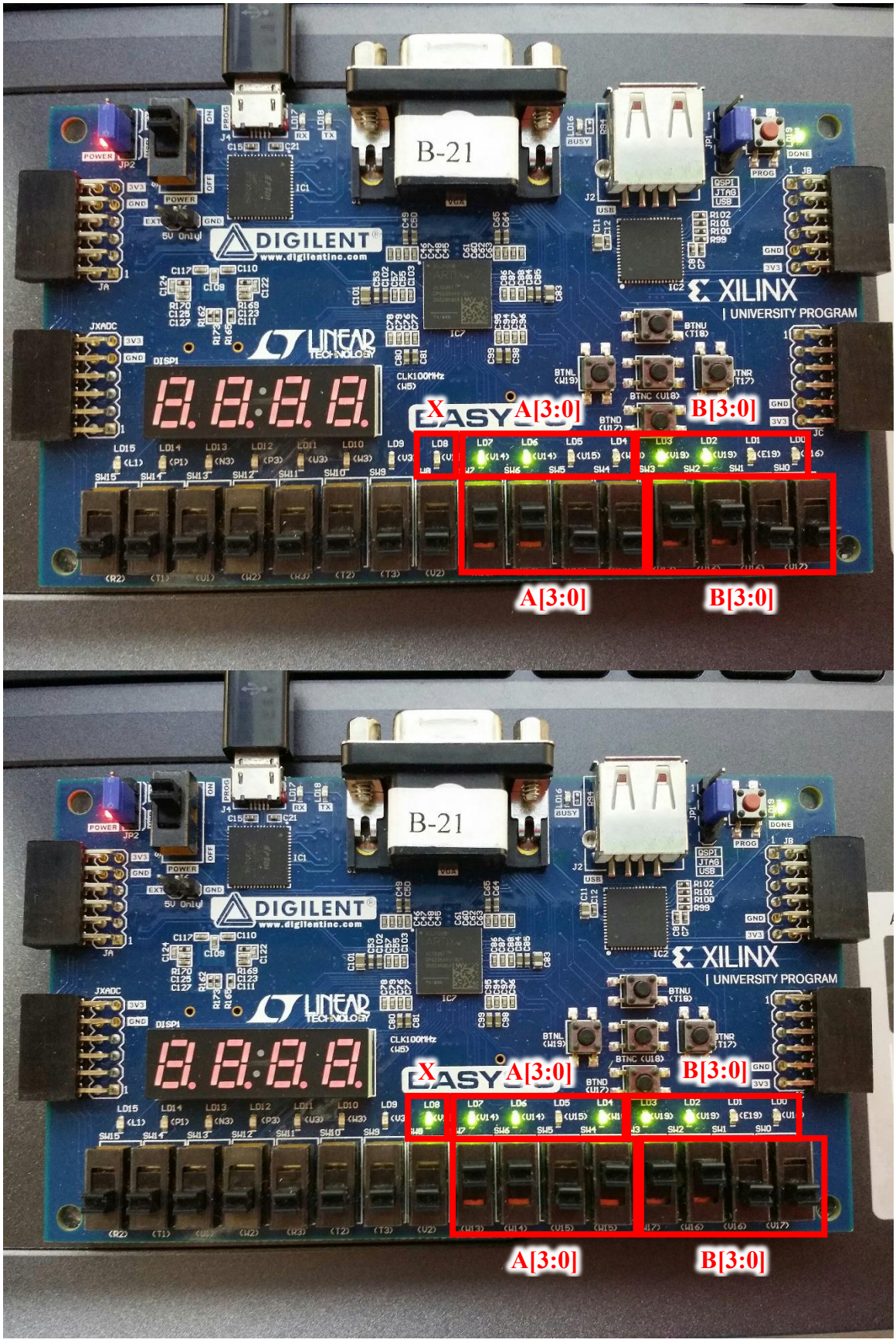
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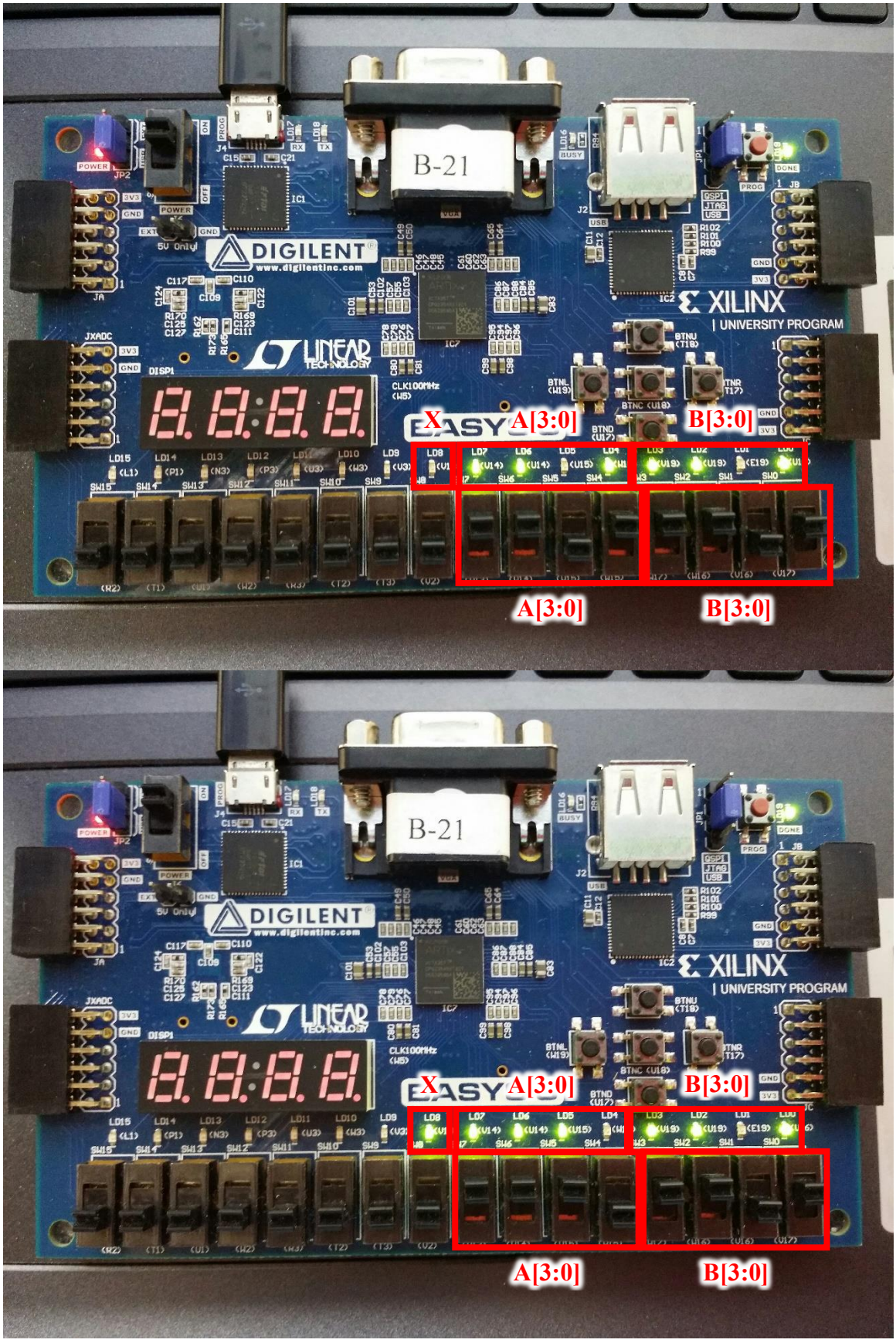
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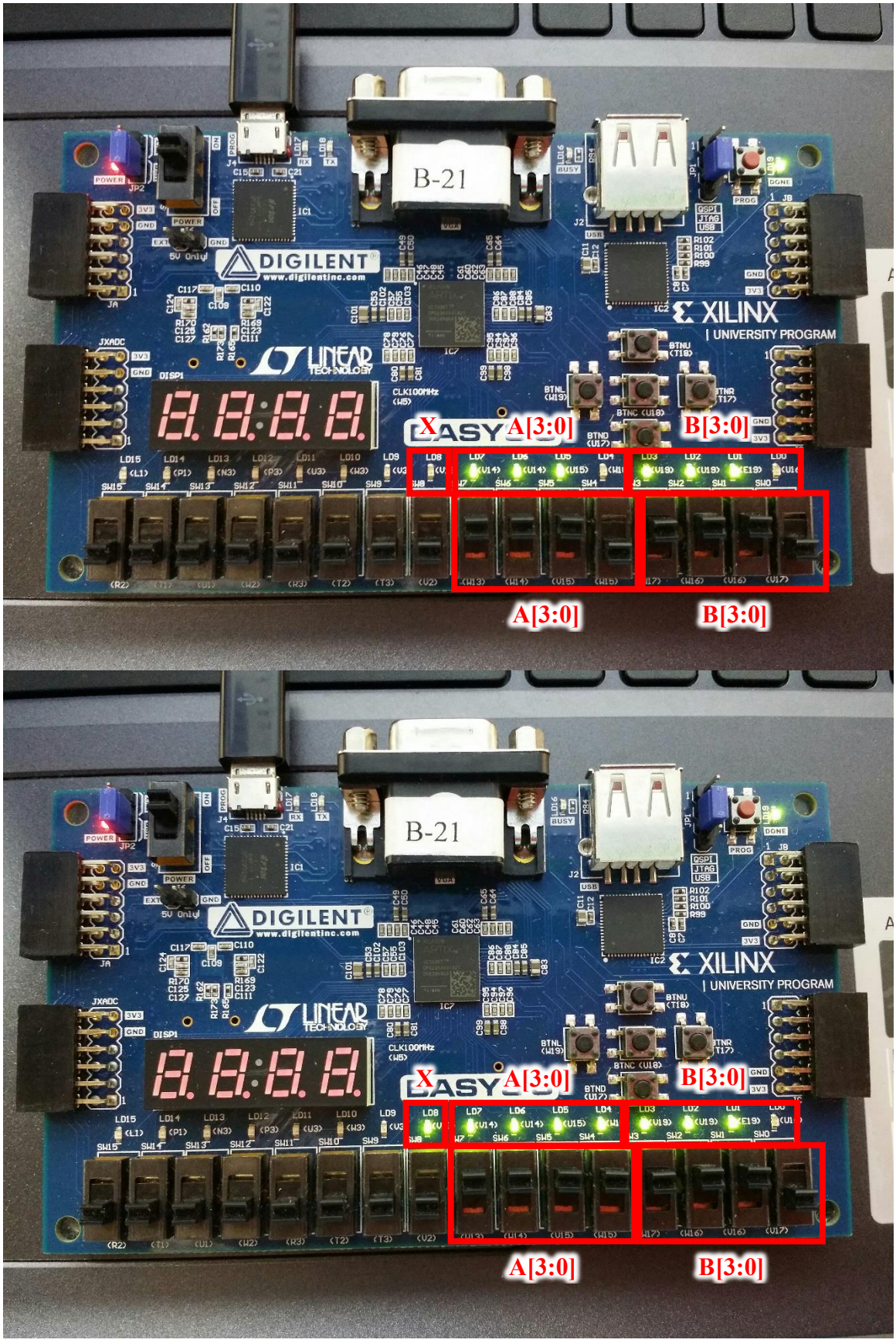
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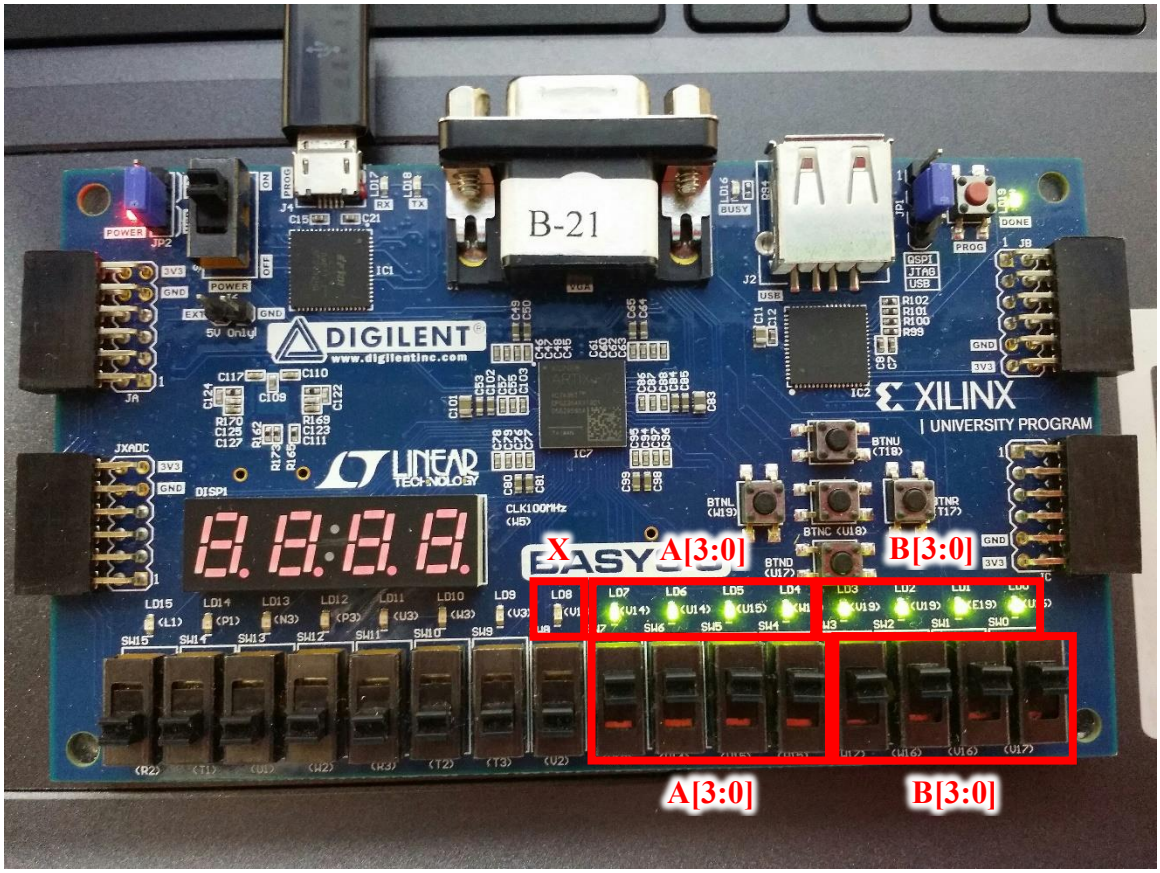

conclusion:

本次 LAB2 實作了加法器、七段顯示器、比較器等電路。與單純在螢幕上看到的 testbench 模擬波型圖比較起來，實際動手操作開關並觀察 LED 與七段顯示器等過程更真實、也更親近電路板。有了 LAB1 的基礎操作經驗之後，本次 LAB2 的 FPGA 操作練習過程十分順利。期待在接下來的數個 LAB 中學習到更多邏輯設計的實作經驗。