Lab 1: Introduction to Verilog HDL

Objective

✓ Review fundamental logic components.
✓ Introduce Verilog HDL modeling and verification.

Prerequisite

✓ Fundamentals of logic gates.

Experiments

1 Design and implement a full adder. ($s+cout=x+y+cin$)
 1.1 Write the logic equation.
 1.2 Draw the related logic diagram.
 1.3 Verilog RTL representation with verification.

2 Design a 3-to-8-line decoder with enable (input in[2:0], enable en and output d[7:0]).
 2.1 Logic equation,
 2.2 Logic schematic,
 2.3 Verilog RTL representation with verification.

3 For two 3-bit unsigned numbers a ($a_2a_1a_0$)and b ($b_2b_1b_0$), build a logic circuit to output the larger number.

4 (Bonus) Design a single digit decimal adder with input A($a_3a_2a_1a_0$), B($b_3b_2b_1b_0$), C_{in}(ci), and output S($s_3s_2s_1s_0$) and C_{out}(co).

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