



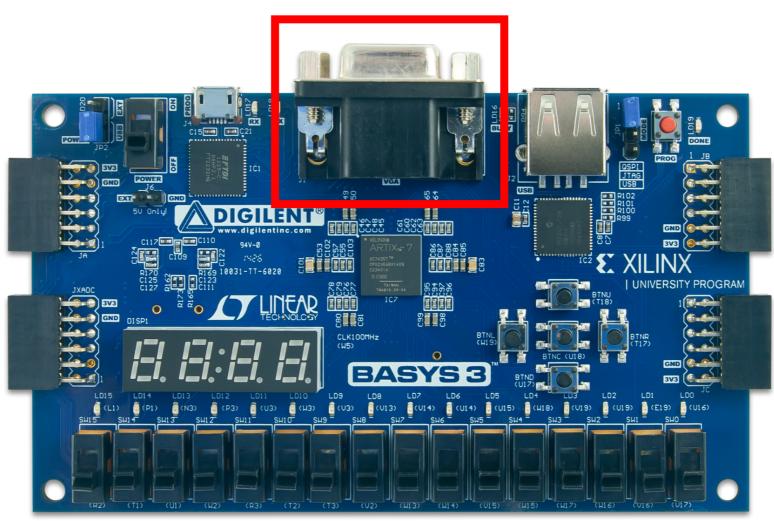
#### Hsi-Pin Ma

http://lms.nthu.edu.tw/course/43639 Department of Electrical Engineering National Tsing Hua University



#### VGA Port

#### VGA

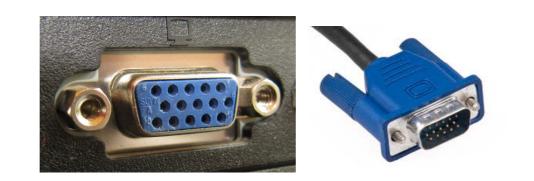




#### VGA

- VGA = Video Graphics Array
- Introduced by IBM in 1987, and still used today
- Transmitting analog signal







Cathode-Ray Tube Monitor

Video Graphics Array DE-15 female and male connector

LED Monitor

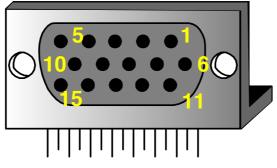


# VGA Video Signal

#### • A VGA video signal contains 5 active signals (RGBHV)

- horizontal sync (HS): used for video synchronization in the horizontal direction
- vertical sync (VS): used for video synchronization in the vertical direction
- red (R): used to control the red color, 0v (fully off)  $\sim 0.7v$  (fully on)
- green (G): used to control the green color, 0v (fully off) ~ 0.7v (fully on)

Basys 3 bibles (Bard Reference Manuarol the blue color, 0v (fully off) ~ 0.72 bidly en on)



Pin 1: Red	Pin 5: GND
Pin 2: Grn	Pin 6: Red GND
Pin 3: Blue	Pin 7: Grn GND
Pin 13: HS	Pin 8: Blu GND
Pin 14: VS	Pin 10: Sync GND
	,



# **Basys 3 Control Signals for VGA**

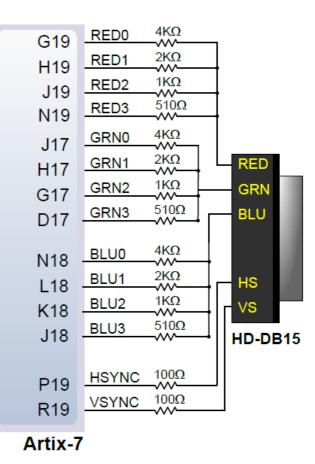
#### • 14 FPGA pins

#### -4-bits per color (R, G, B)

-2 standard sync signals (HS, VS)

#### ##VGA Connector

set property PACKAGE PIN G19 [get ports {vgaRed[0]}] set property IOSTANDARD LVCMOS33 [get ports {vgaRed[0]}] set property PACKAGE PIN H19 [get ports {vgaRed[1]}] set property IOSTANDARD LVCMOS33 [get ports {vgaRed[1]}] set property PACKAGE PIN J19 [get ports {vgaRed[2]}] set property IOSTANDARD LVCMOS33 [get ports {vgaRed[2]}] set property PACKAGE PIN N19 [get ports {vgaRed[3]}] set property IOSTANDARD LVCMOS33 [get ports {vgaRed[3]}] set property PACKAGE PIN N18 [get ports {vgaBlue[0]}] set property IOSTANDARD LVCMOS33 [get ports {vqaBlue[0]}] set\_property PACKAGE\_PIN\_L18 [get\_ports {vgaBlue[1]}] set property IOSTANDARD LVCMOS33 [get ports {vgaBlue[1]}] set property PACKAGE PIN K18 [get ports {vgaBlue[2]}] set property IOSTANDARD LVCMOS33 [get ports {vgaBlue[2]}] set property PACKAGE PIN J18 [get ports {vgaBlue[3]}] set property IOSTANDARD LVCMOS33 [get ports {vgaBlue[3]}] set property PACKAGE PIN J17 [get ports {vgaGreen[0]}] set property IOSTANDARD LVCMOS33 [get ports {vgaGreen[0]}] set property PACKAGE PIN H17 [get ports {vgaGreen[1]}] set property IOSTANDARD LVCMOS33 [get ports {vqaGreen[1]}] set\_property PACKAGE\_PIN G17 [get\_ports {vgaGreen[2]}] set property IOSTANDARD LVCMOS33 [get ports {vgaGreen[2]}] set property PACKAGE PIN D17 [get ports {vgaGreen[3]}] set property IOSTANDARD LVCMOS33 [get ports {vgaGreen[3]}] set property PACKAGE PIN P19 [get ports hsync] set property IOSTANDARD LVCMOS33 [get ports hsync] set property PACKAGE PIN R19 [get ports vsync] set property IOSTANDARD LVCMOS33 [get ports vsync]



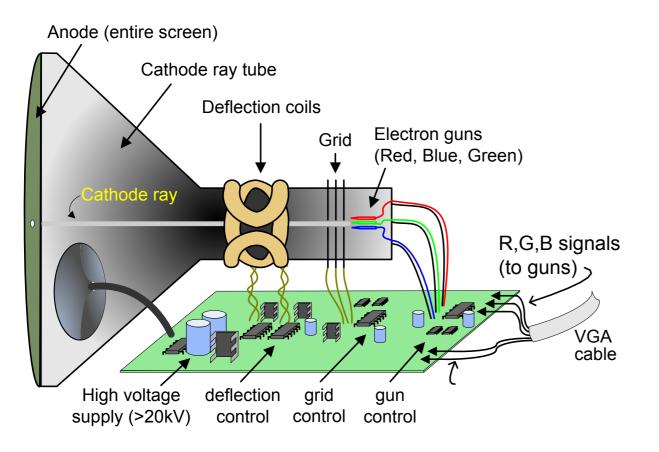




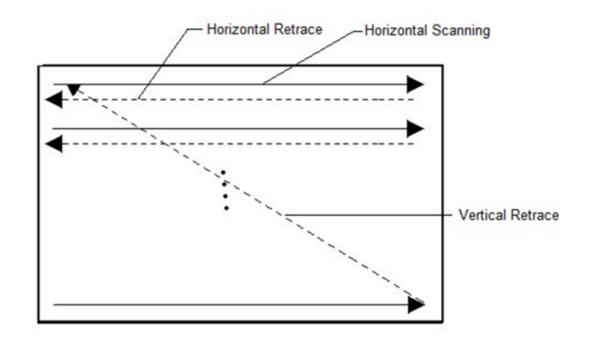
• Cathode Ray Tube (CRT) is a vacuum tube containing one or more electron guns, and a phosphorescent screen is used to view images.



#### GA Board Reference Manual



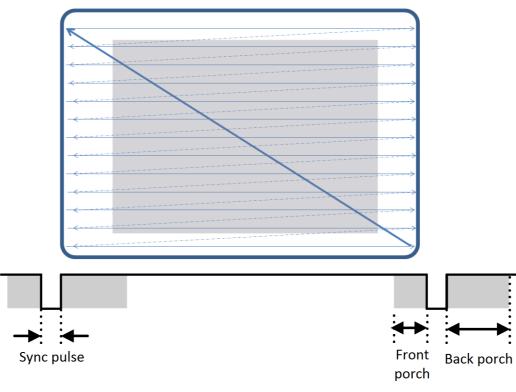
#### 





# VGA System Timing (1/3)

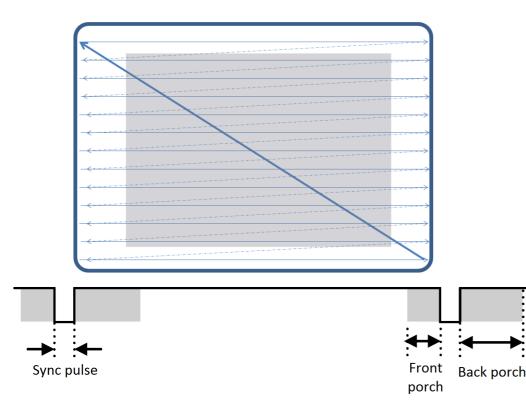
- Whether the information is displayed
  - Displayed: beam moving forward (left to right and top to bottom)
  - -Not displayed: the time the beam is reset back to the left or top edge of the display. (Blanking period)
- Display resolution is determined by
  - the size of the beams
  - the frequency at which the beam can be traced across the display
  - the frequency at which the electron beam can be modulated

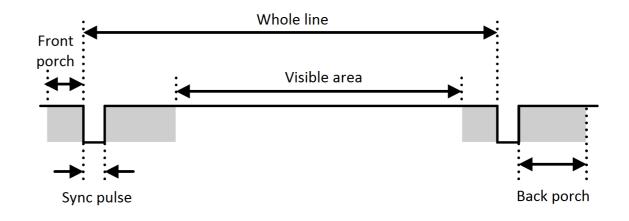




# VGA System Timing (3/3)

• Signal timing for a 640-pixel by 480 rows display using a 25MHz pixel clock





Parameter	Ver. Sync		Hor. Sync	
	Lines	Time(ms)	Pixels	Time(µs)
Visible area	480	15.3	640	25
Front porch	10	0.3	16	0.64
Sync pulse	2	0.064	96	3.8
Back porch	33	1.05	48	1.9
Whole line	525	16.7	800	32



### Pixel Clock

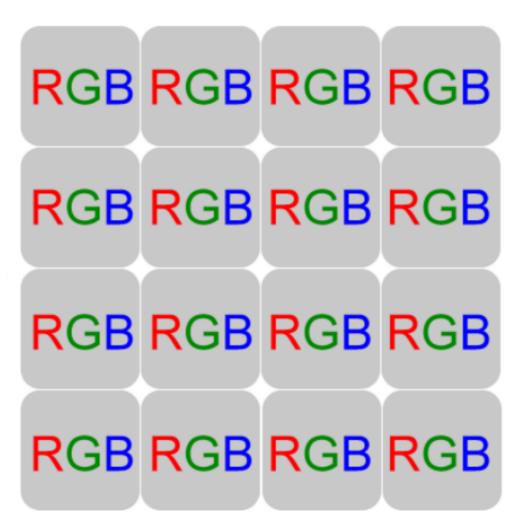
- The pixel clock defines the time available to display one pixel of information.
- Example: Suppose we want to display an image with 480 rows and 640 columns, and its refresh rate is 60Hz. The pixel clock which will be delivered to VGA screen must be

800\*525\*60(frame/sec) = 25M (pixel/sec)



# **RGB Bitmap**

- A digital color image is composed by a lot of pixels.
- Each pixel contains three R, G, B values to represent the intensity of these three primary colors.



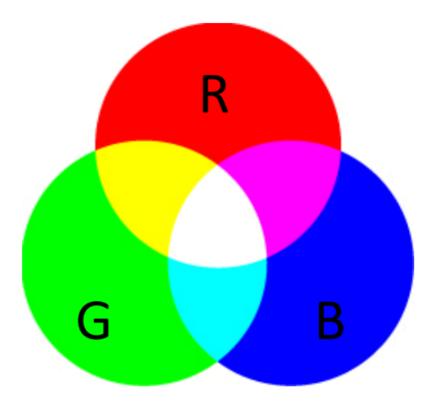
# **RGB Color Mode**

- Three primary colors
  - -Red

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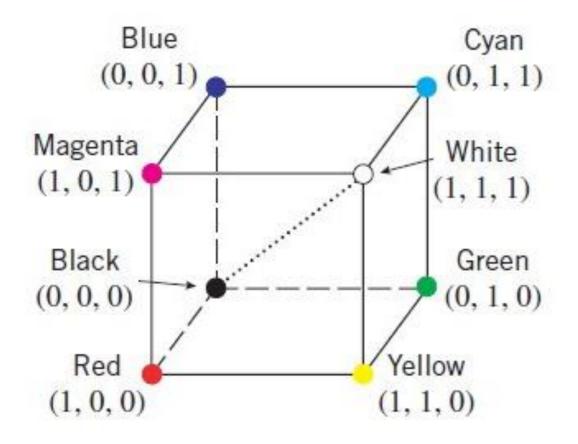
- -Green
- -Blue
- No one of them can be created as the other two.
- Any other color is a combination

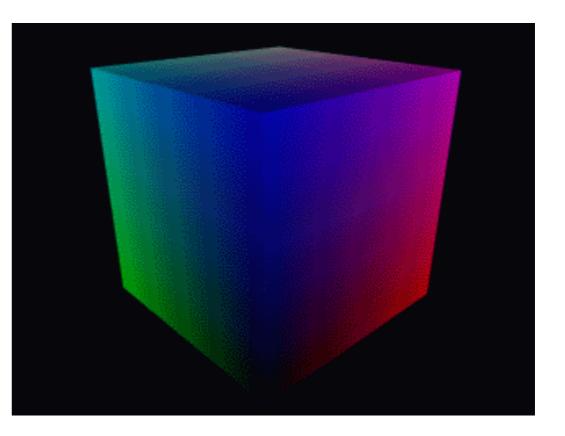




## **RGB Color Cube**

- R, G, and B correspond to three axes in 3D space.
- Normalize the relative amounts of R, G and B so that each value varies between 0 and 1.



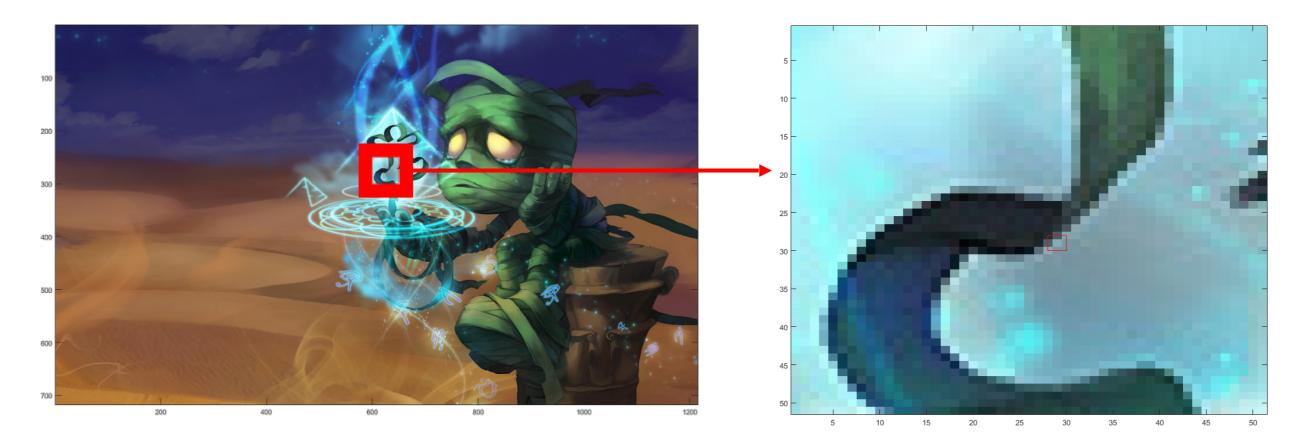




### RGB Bitmap Example (1/2)

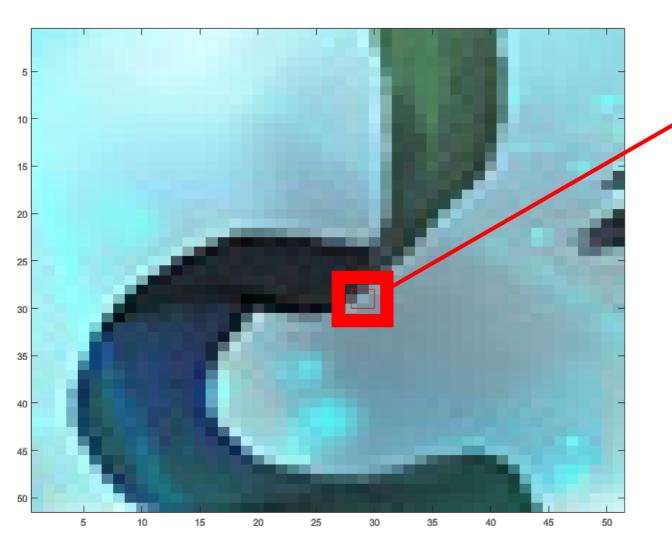
Size: 1215\*717

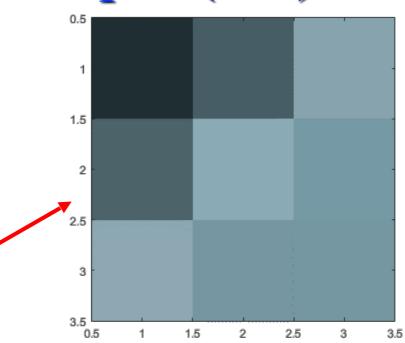
Size: 51\*51





# RGB Bitmap Example (2/2)





#### (R,G,B) : range from 0 to 255

(31,46,51)	(70,93,101)	(135,163,174)
(76,99,105)	(138,170,181)	(117,153,165)
(141,168,179)	(118,150,161)	(117,151,161)



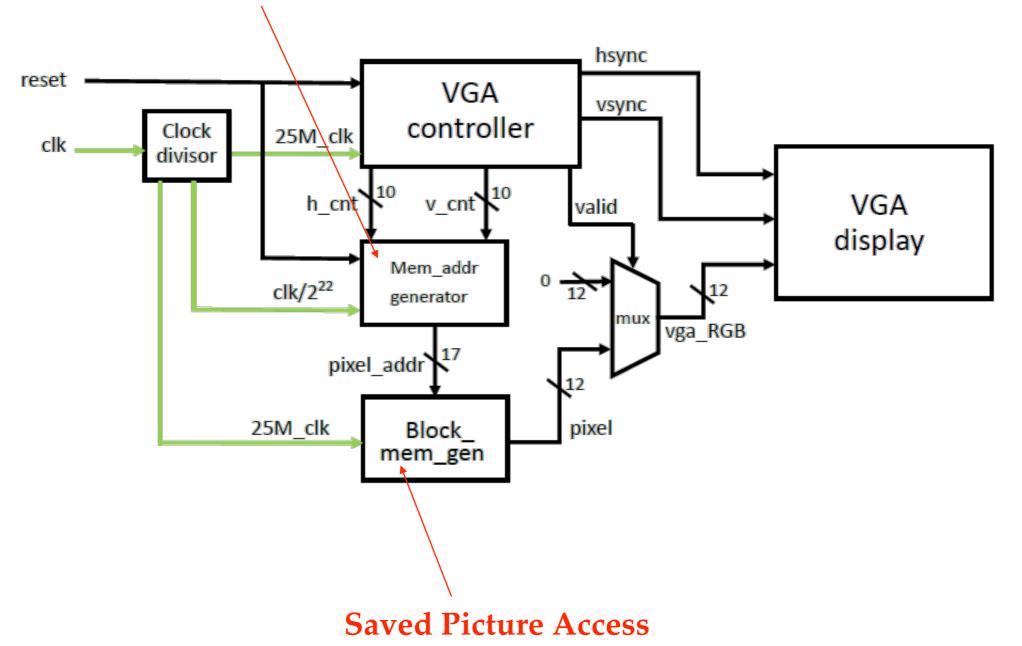
#### Demo 1: Block Diagram

#### Тор hsync reset -VGA vsync controller Clock 25M\_clk clk divisor h\_cnt <sup>10</sup> v\_cnt <sup>10</sup> VGA valid display 12 Pixel vga\_RGB generator



## Demo 2: Block Diagram

#### reduce the resolution from 640x480 to 320x240





# Memory IP (1/5)



2.							
Searc]	h: Q- memory	(20	) matches)				
a Name		^1	AXI4	Status	License	VLNV	
8 🖃 🕞	Vivado Repository						
- -	🕞 AXI Infrastructure						
	🚽 📑 AXI Central Dire	ect Memory Access	AXI4	Production	Included	xilinx.com:ip	
	📲 🕂 AXI Direct Mem	ory Access	AXI4, AXI4-Stream	Production	Included	xilinx.com:ip	
	📲 AXI Memory M	apped to Stream Mapper	AXI4, AXI4-Stream	Production	Included	xilinx.com:ip	
ţ	📭 📭 AXI Video Direc	t Memory Access	AXI4, AXI4-Stream	Production	Included	xilinx.com:ip	
<u>ا</u>	🕞 Basic Elements	3					
	📄 🕞 Memory Elemen						
	🚽 📴 Block Memo	ry Generator	AXI4	Production	Included	xilinx.com:ip	
]	- Distributed in	temory Generator		Production	Included	xilinx.com:ip	
	Communication 9 Networking						
2	🖻 🕞 Ethernet						
1	🖳 📴 AXI Direct M	lemory Access	AXI4, AXI4-Stream	Production	Included	xilinx.com:ip	
-	📄 Embedded Processin	ıg					
	🚊 🕞 AXI Infrastructu	re					
	🚽 📑 AXI Memory	Mapped to Stream Mapper	AXI4, AXI4-Stream	Production	Included	xilinx.com:ip	
	🖻 🕞 DMA						
	🚽 📑 AXI Cent	ral Direct Memory Access	AXI4	Production	Included	xilinx.com:ip	
	🚽 📭 AXI Direc	t Memory Access	AXI4, AXI4-Stream	Production	Included	xilinx.com:ip	
	📑 🕂 🕂 🕂 🕂	o Direct Memory Access	AXI4, AXI4-Stream	Production	Included	xilinx.com:ip	
	M						



# Memory IP (2/5)

: Customize IP Slock Memory Generator (8.2)	and the second se		
🖉 Documentation 🛅 IP Location 🧔 Switch to Defaults			
IP Symbol Power Estimation Show disabled ports	Component Name blk_mem_gen_1 Basic Port & Options Other Options Summary		
	Interface Type Native     Generate address interface with 32 bits     Memory Type Single Port RAM		Memory Type Single Port RAM
	ECC Options ECC Type No ECC *		
	Error Injection Pins Single Bit Error Injection		
	Write Enable		BRAM_PORTA
BRAM_PORTA	Byte Size (bits) 9		→addra[16:0]
■ BRAM_PORTA ■ addra[16:0]	Algorithm Options Defines the algorithm used to concatenate the block RAM primitives. Refer datasheet for more information.		
- Cika	Algorithm Minimum Area - Primitive 80x2 -		- Clka
dina[11:0]			- dina[11:0]
→wea[0:0]			
			wea[0:0]
۴ ۴	-	OK Cancel	



# Memory IP (3/5)

Block Memory Generator (8.2)	Customize IP	
Pocuenciation P Location & Switch to Default      Psymbol Fover Estimation     Show disabled ports      Besic Port A Options Other Options Summary      Memory Size      Write Width 12 Read; 11 to 4608 (bits)     Read Width, 12 Read; 21 to 4608 (bits)     Read Width, 12 Read; 21 to 4608 (bits)     Read Width, 12 Read; 22 to 1048576     Read Depth 76800 Read; 22 to 1048576     Read Depth 76800 Read; 22 to 1048576     Read Depth 76800	lock Memory Generator (8.2)	Component Name blk_mem_gen_0
IP Symbol       Power Estimation         In the Wath       Internet to the Wath         Internet to the Wath       I	Documentation 🛅 IP Location 🧔 Switch to Defaults	
Memory Size         Write Width       12         Write Width       12         Write Depth       76800         Read Depth       76800         Operating Mode       Write First * Enable Port Type         Use ENA Fin       Use ENA Fin         Use ENA Fin       Use ENA Fin         Use ENA Fin       Core Outhul Register:         Use ENA Fin       Core Outhul Register:	IP Symbol Power Estimation Commonent Name bik mem sen 1	
Memory Sze       Write Width 12       Ra. ge: 1 to 4608 (bits)         Read Width 12       Write Width 12       Ra. ge: 1 to 4608 (bits)         Write Depth 76800       Range: 2 to 1048576       Read Width 12         Read Width 76800       Range: 2 to 1048576       Range: 2 to 1048576         Operating Mode Write Furst width 76800       Range: 2 to 1048576         Port A Optional Output Register:       Newsy: Enabled         Use ENA Fra       Use ENA Fra         Write Register:       Core Output Register:         Primitives Output Register:       Core Output Register:	Show disabled ports Basic Port A Options Other Options Summary	Nemona Size
Read Width 12 Write Depth 76800 Read Depth 76800 Operating Mode Write First  Enable Port Type Use ENA Pin  Port A Optional Output Registers Use ENA Pin  Use E	Memory Size	Tentory Size
Read Width 12 Write Depth 76800 Read Depth 76800 Operating Mode Write First  Enable Port Type Use ENA Pin Port A Optional Output Register  Core Output	Write Width 12 S Range: 1 to 4608 (bits)	Write Width 12 Range: 1 to 4608 (bits)
Read Depth 76800 Operating Mode Write First  Enable Port Type Use ENA Pin  Port A Optional Output Registers Use ENA Pin Use E	Read Width 12 -	
Operating Mode Write First   Enable Port Type Use ENA Pin   Port A Optional Output Registers Always Enabled   Use ENA Pin     Write Depth     76800     Read Depth     76800		Read Width 12 V
Operating Mode Write First  Enable Port Type Use ENA Pin Port A Optional Output Registers Use ENA Pin Use ENA Pin Operating Core Output Register	Read Depth 7 <u>76800</u>	Wyite Denth 76800 🔗 Rative: 2 to 1048576
Port A Optional Output Registers Always Enabled Use ENA Pin Primitives Output Register Core Output Register		
Use ENA Pin		Read Depth [76800
	Use ENA Pin	
BRAM_PORTA Operating Mode Write First - Enable Port Type Always Enabled		
	BRAM_PORTA SoftECC Input Register REGCEA Pin	Operating Mode 🛛 Write First 👻 Enable Port Type Always Enabled 💌
Addra[16:0] Port & Output Reset Options	Port & Output Reset Options	
P PT A Dir (athenet sin) Otherst Reset Value (Hava)	E BSTA Bin (athrest sin) Output Bout Value (Lev) 0	
Clka     Reset Memory Latch     Reset Priority     CE (Latch or Register Enable)	Reset Memory Latch Reset Priority CE (Latch or Register Enable) -	
→ dina[11:0]	- • dina[11:0]	
- douta[11:0] READ Address Change A	- douta[11:0] READ Address Change A	
− ▶wea[0:0] RGB : 12 bits		$\mathbf{RGR} \cdot 12$ hits
		<b>ROD</b> . 12 01t5
320x240:76800		$320 \times 240 \cdot 76800$
J20A240.70000		J20A2TU. /0000
۲	۲ ( ۲ ) ۲ ( ) 1 (	
OK Cancel		OK Cancel

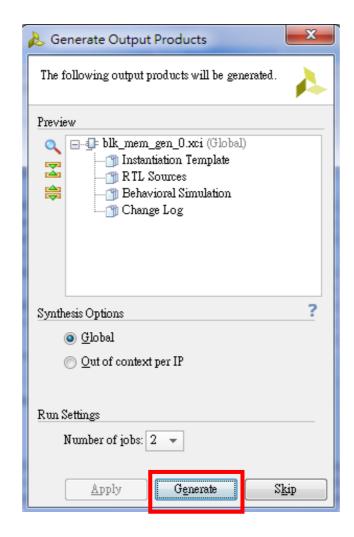
1800kbits of fast block RAM in FPGA



# Memory IP (4/5)

Get Customize IP	and a second secon	<b>X</b>		
Block Memory Generator (8.2)				
🍘 Documentation 📄 IP Location 🧔 Switch to Defaults				
IP Symbol Power Estimation	ComponentName blk mem sen 1	۲		
Show disabled ports	Basic Port & Options Other Options Summary		Component Name blk_mem_gen_0	
	Pipeline Stages within Mux 0 - Mux Size: 19x1 Memory Initialization		Basic Port A Options Other Options Summary	
	V Load Init File		Pipeline Stages within Mux 0	
	Coe File no_coe_file_loaded		Memory Initialization	2. Choose .coe file
			🔽 Load Init File	
	Fill Remaining Memory Locations Remaining Memory Locations (Hex) 0			
	Structural/UniSim Simulation Model Options		Coe File no_coe_file_loaded	Browse 📝 Edit
BRAM_PORTA	Defines the type of warnings and outputs are generated when a read-write or write-write collision occurs.			
→addra[16:0]	Collision Warnings All			
- Clka	Behavioral Simulation Model Options			
dina[11:0]	Disable Collision Warnings Disable Out of Range Warnings			
douta[11:0]				
wea[0:0]				
	3			
<	J			
		Cancel		

# Memory IP (5/5)



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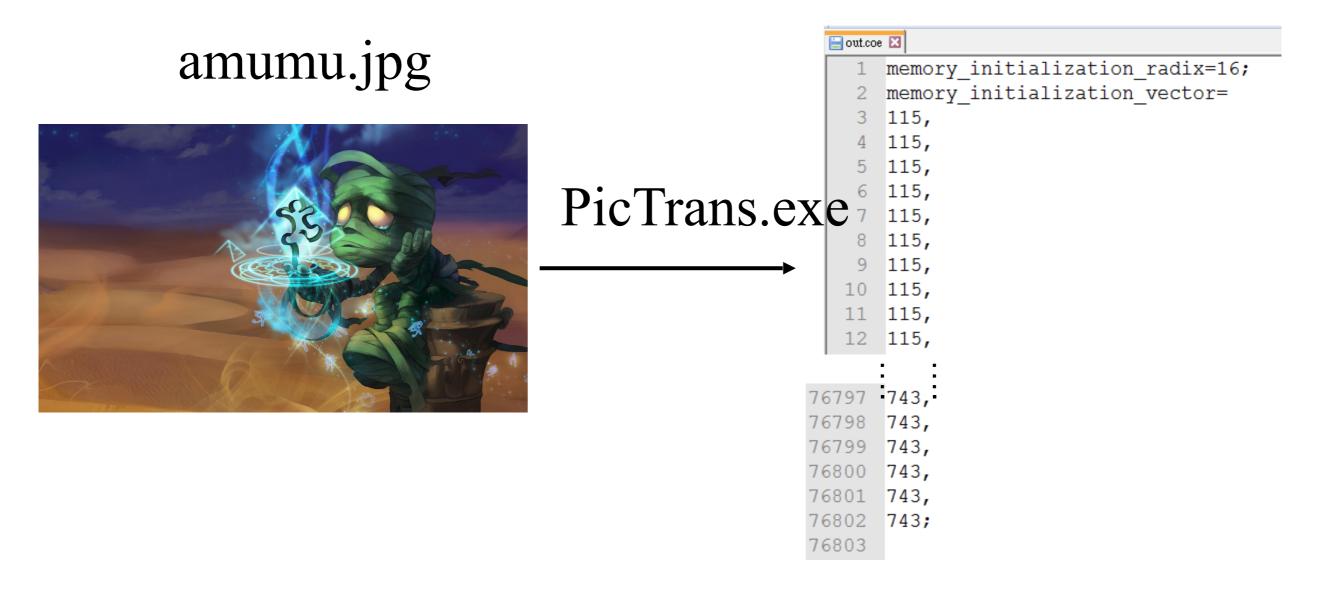
Computing

NTHU EE



## Picture Format Translation (1/2)

#### out.coe





# Picture Format Translation (2/2)

#### • PicTrans.exe:

-Convert a \*.jpg file to a bit map file

#### • Input:

- -image (\*.jpg)
- the width of the output file
- the height of the output file

### • Output:

-out.coe





# Lab 11: VGA Display



# Action Item (1/2)

Modify the Verilog code introduced in class to design a circuit for controlling the VGA display.

• input ports:

input clk; input reset; input en;

#### • output ports:

output [3:0]vgaRed; output [3:0]vgaGreen; output [3:0]vgaBlue; output hsync; output vsync;



# Action Item (2/2)

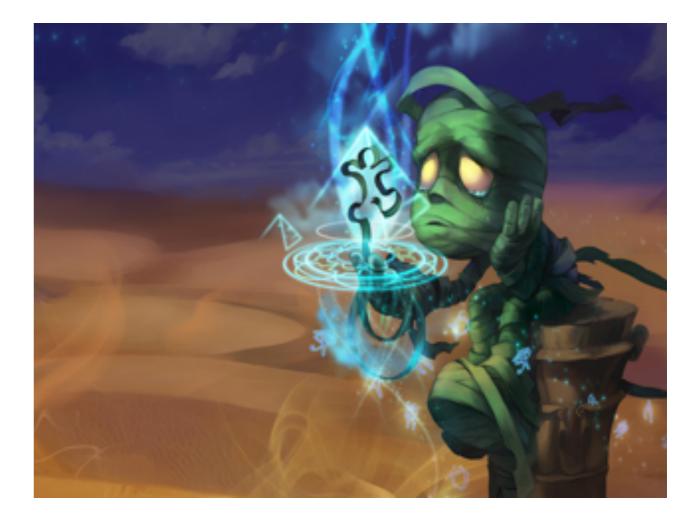
- At the beginning or when pressing the **reset** button, the VGA display will show the image (e.g., amumu.jpg) at the origin position. It will stay still until the **en** button is pressed.
- The image will start/resume scrolling down row by row under the frequency of clk divided by 2<sup>22</sup> (i.e., clk/2<sup>22</sup>), or pause, depending on whether the number of the **en** button pressed is odd or even.



# Example (1/6)

#### at the beginning or pressing reset

#### (0 row scrolled down)

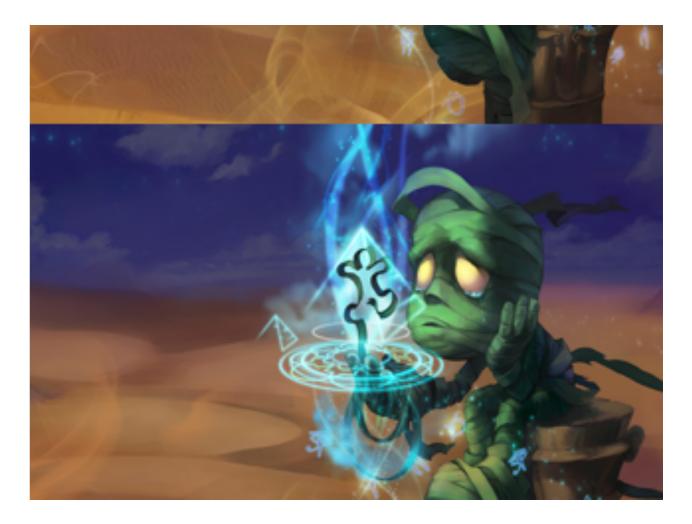




# Example (2/6)

#### press en $\rightarrow$ start to scroll down

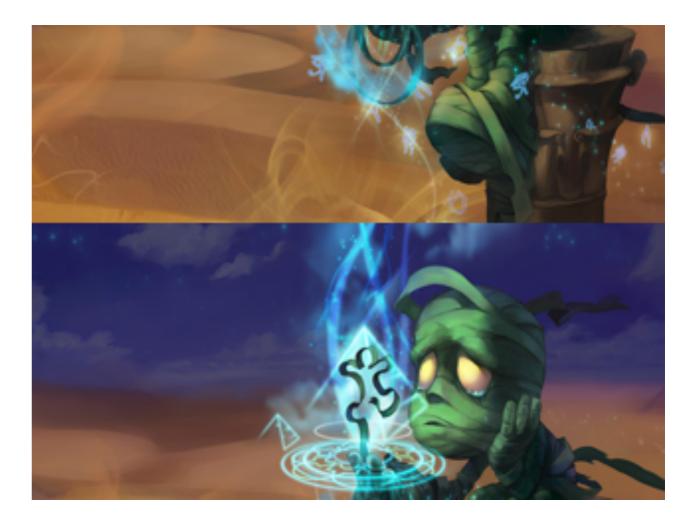
#### (100 rows scrolled down)





#### Example (3/6)

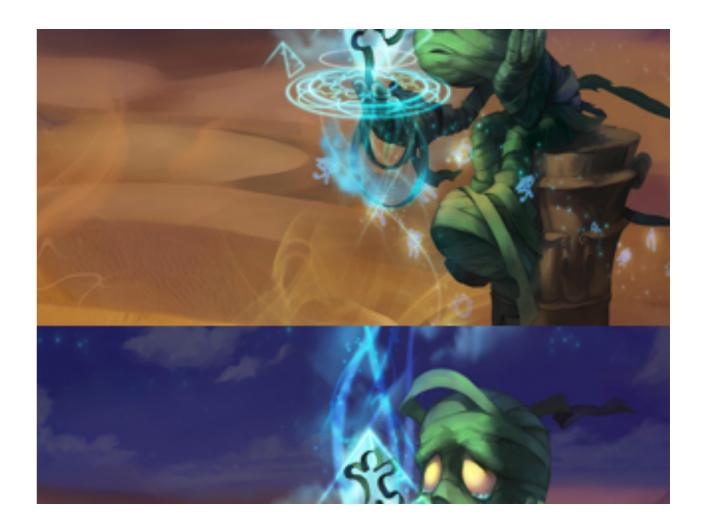
#### (200 rows scrolled down)





#### Example (4/6)

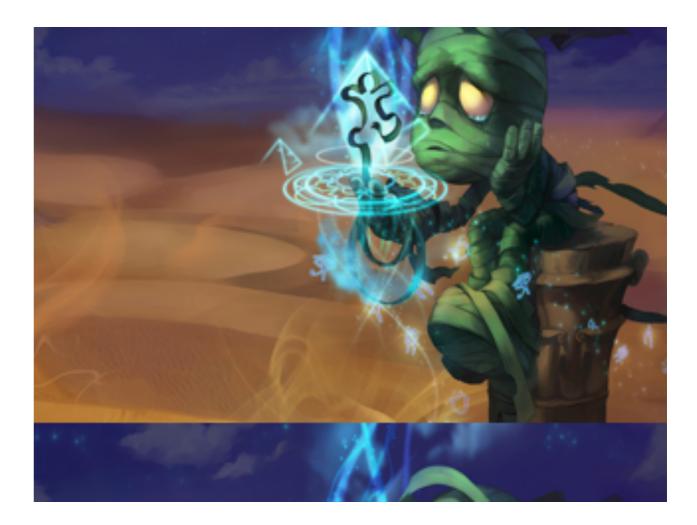
#### (300 rows scrolled down)





#### Example (5/6)

#### (400 rows scrolled down)





### Example (6/6)

#### press en pause

#### (400 rows scrolled down)

