

# FPGA Emulation

Hsi-Pin Ma

<http://lms.nthu.edu.tw/course/43639>

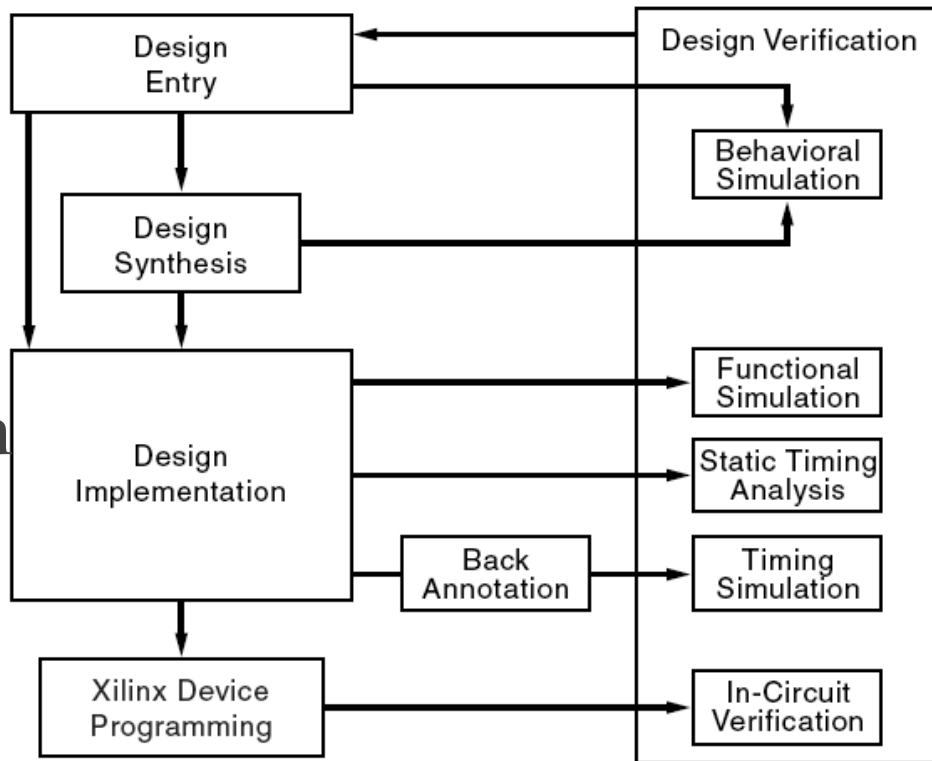
Department of Electrical Engineering  
National Tsing Hua University

# Notes from Lab1

- Always 'SAVE' before next step
- Select the right file for the next step
  - For simulation
  - For implementation
- Do not use specific names for files and directories
  - Leading with number,
  - Names with space,
  - Names in Chinese

# Design Flow

- General design flow
  - Design construction
  - Behavioral simulation
  - Design implementation
  - Timing simulation
- HDL-based design Flow



# Important Notes

- **Draw schematic first** and then construct Verilog codes.
- Verilog RTL coding philosophy is not the same as C programming
  - Every Verilog RTL construct has its own logic mapping (for synthesis)
  - You should have the logics (draw schematic) first and then the RTL codes
  - You have to write **synthesizable** RTL codes

# Digilent Basys 3 Demo Board

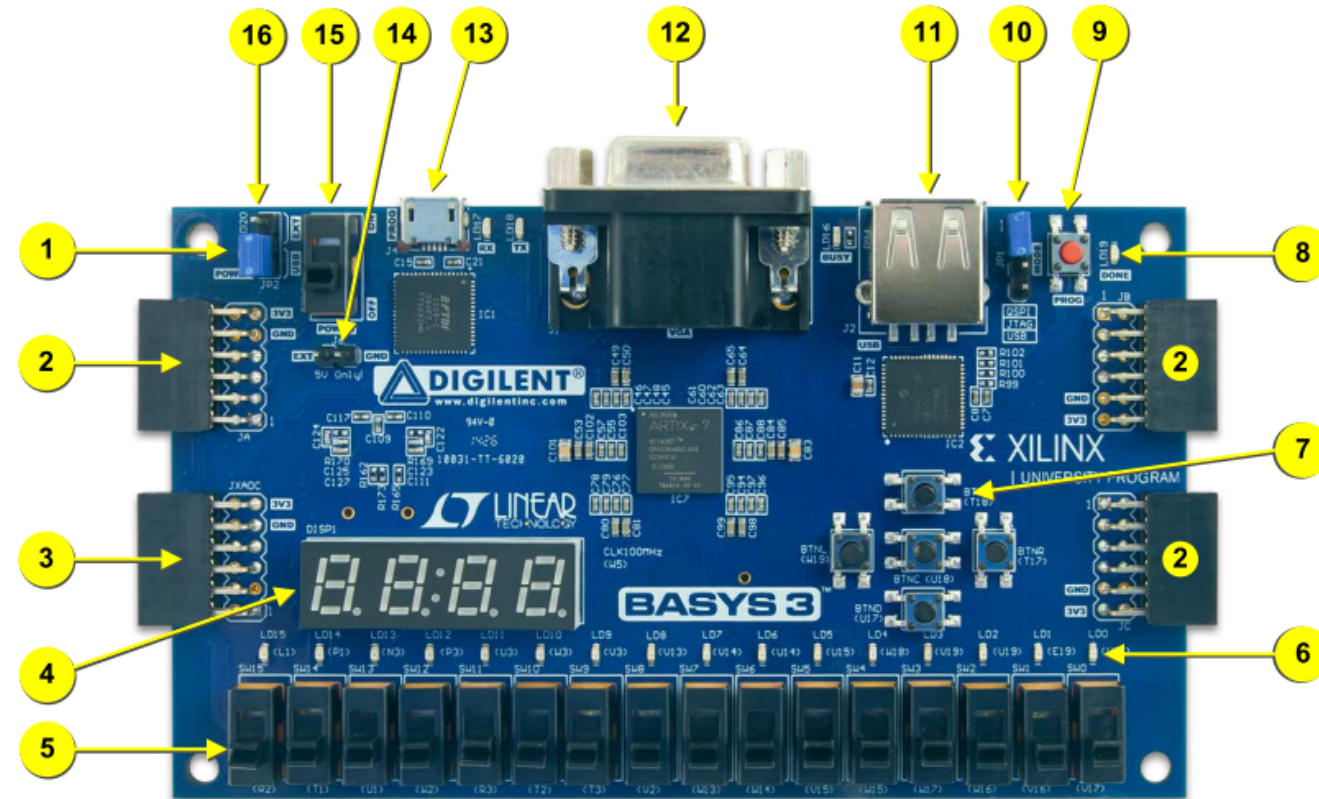


Figure 1. Basys3 FPGA board with callouts.

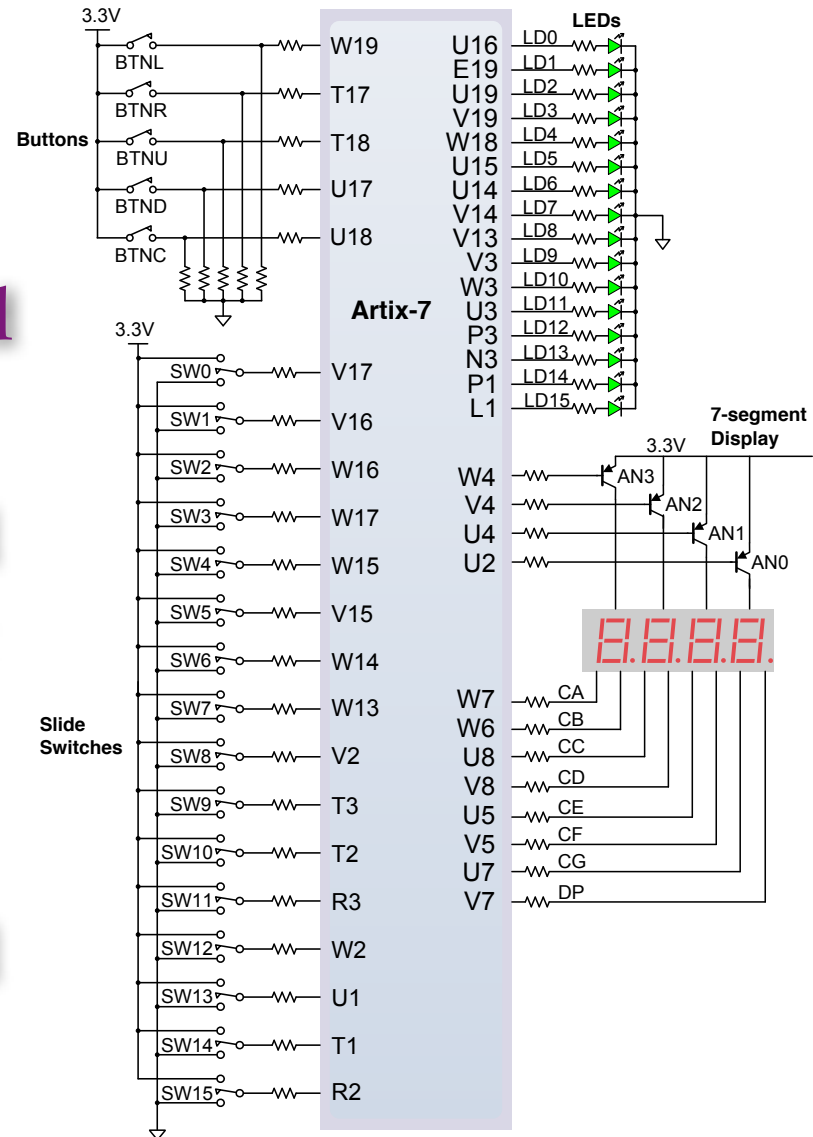
Callout	Component Description
1	Power good LED
2	Pmod connector(s)
3	Analog signal Pmod connector (XADC)
4	Four digit 7-segment display
5	Slide switches (16)
6	LEDs (16)
7	Pushbuttons (5)
8	FPGA programming done LED
9	FPGA configuration reset button
10	Programming mode jumper
11	USB host connector
12	VGA connector
13	Shared UART/JTAG USB port
14	External power connector
15	Power Switch
16	Power Select Jumper

<https://reference.digilentinc.com/reference/programmable-logic/basys-3/start?redirect=1>

[Check Basys 3 board reference manual for details](#)

# Input/Output Connections

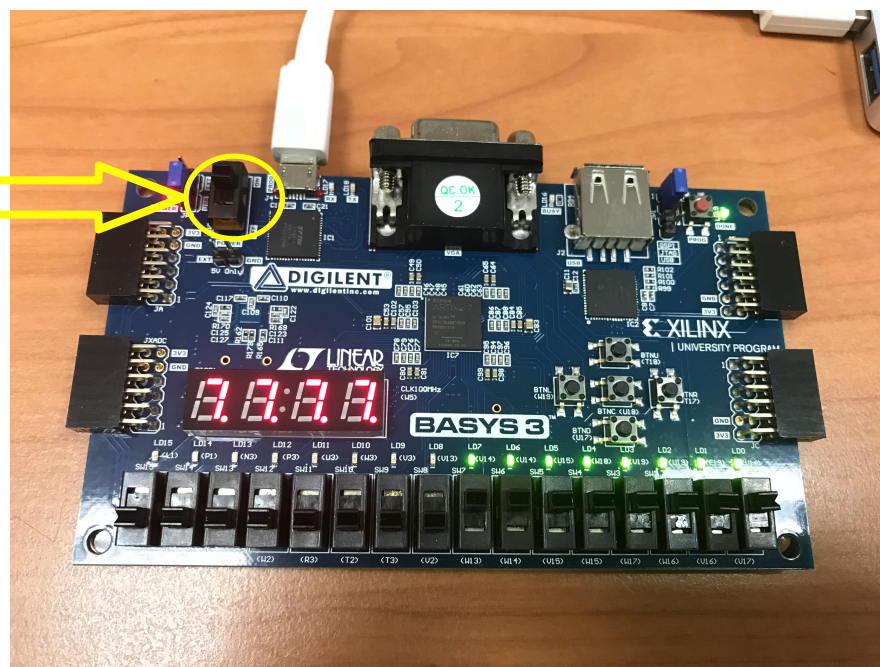
- LEDs are pre-wired **HIGH** active control
- 7-Seg Display are pre-wired **LOW** active control
- Push buttons are pre-wired **LOW** when they are at rest
- DIP switches generate **HIGH** when tuned up and generate **LOW** when tuned down



# Test Your FPGA Board (1/3)

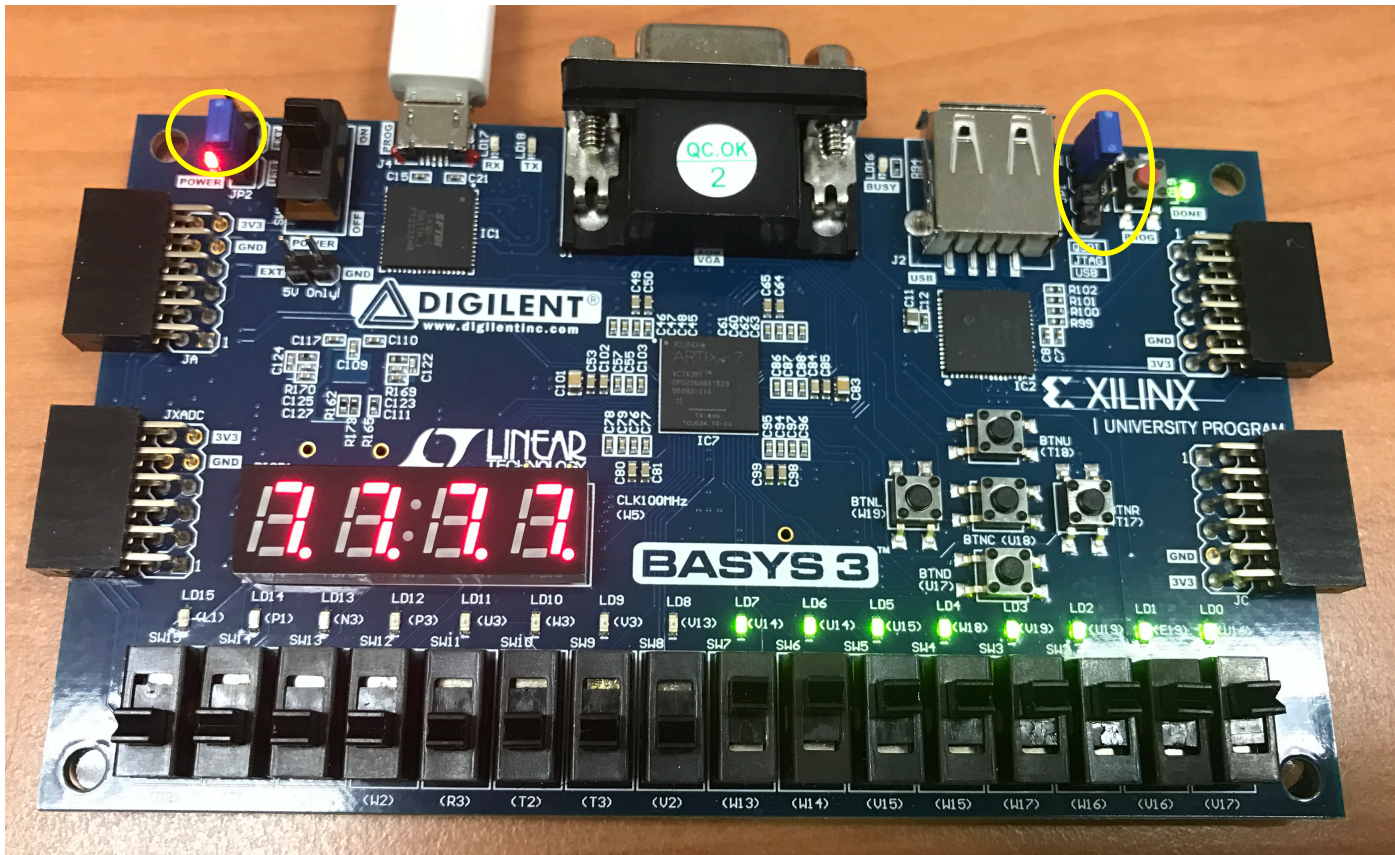
- Connect the demo board to PC and also the power supply

- 所有的線接好再開電源
- 關閉電源後再拔所有的線
- 勿用導體接觸針腳
- 插座別插反了
- 避免長時間開機



# Test Your FPGA Board (2/3)

- Don't move or remove the jumpers

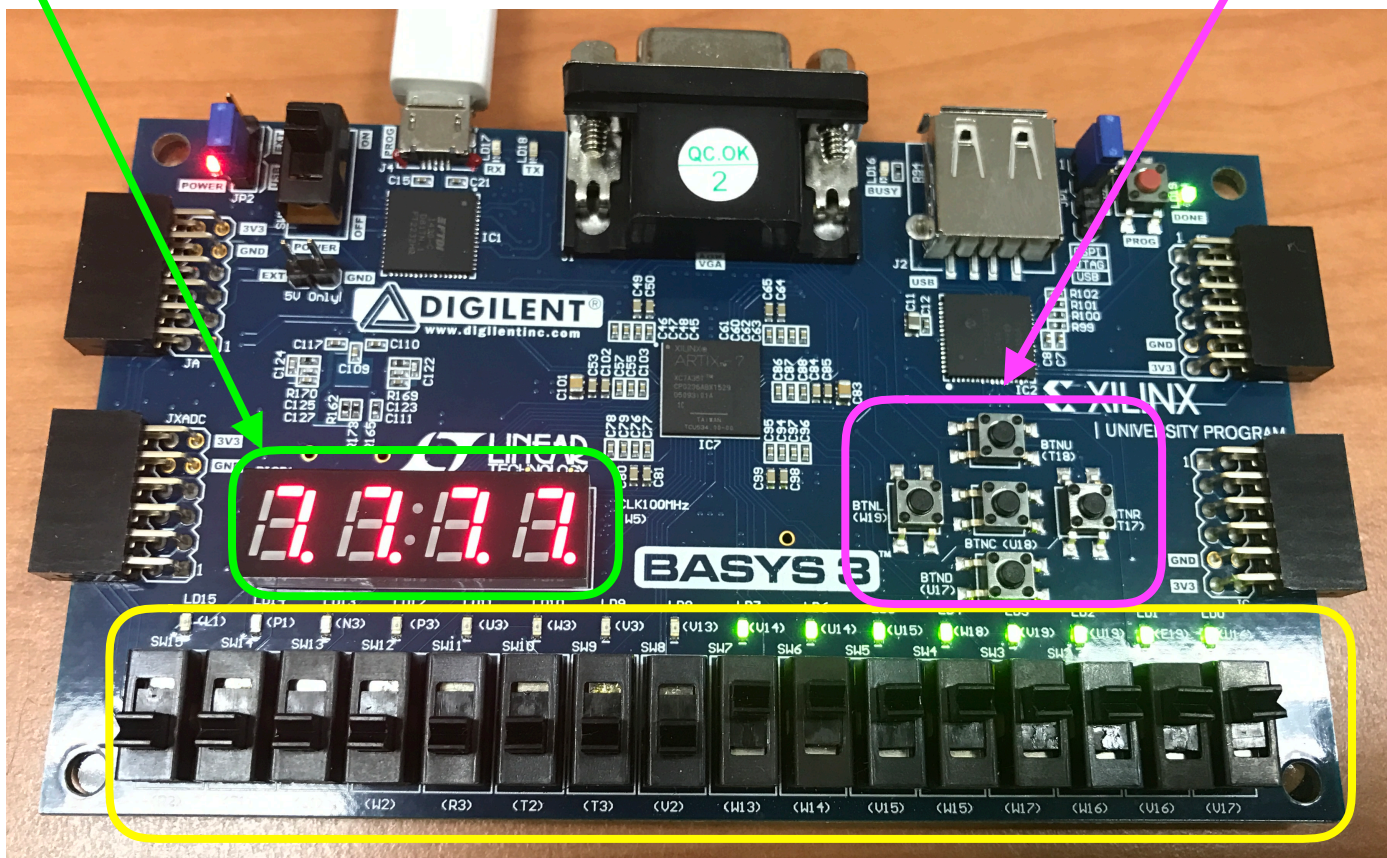




# Test Your FPGA Board (3/3)

BCD counts on 7-Seg Displays continuously

Push buttons control the 7-Seg display



DIP Switch control the LEDs

# FPGA Emulation Using Xilinx Vivado

# Design Flow

- Design Source Preparation
  - Design modules (.v)
  - Design constraints (I/O pin assignments) (.xdc)
- Design Simulation
  - testbench (.v)
- Design Synthesis and Implementation

# Create New Project (2/3)

Continue from previous unit slides

New Project
✕

### Default Part

Choose a default Xilinx part or board for your project. This can be changed later.

Select: Parts Boards

Filter

Product category: All

Family: Artix-7

Package: cpg236

Speed grade: -1

Temp grade: All Remaining

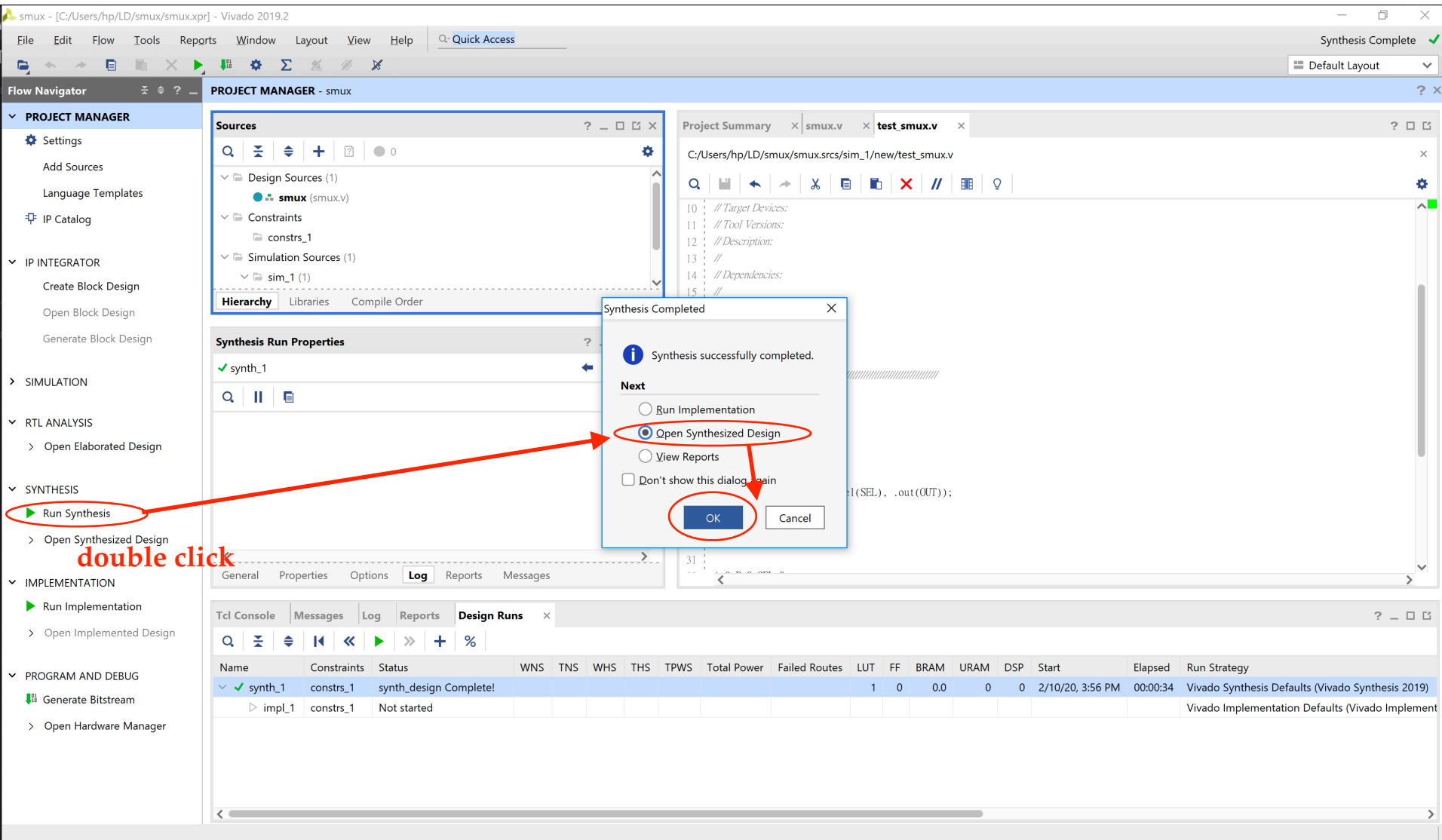
Reset All Filters

Search:  (1 match)

Part	I/O Pin Count	Block RAMs	DSPs	FlipFlops	GTPE2 Transceivers	Gb Transceivers	Available IOBs	LUT Elements
xc7a35tcpg236-1	236	50	90	41600	2	2	106	20800

?
< Back
Next >
Finish
Cancel

# I/O Pins Assignment (1/4)



smux - [C:/Users/hp/LD/smux/smux.xpr] - Vivado 2019.2

File Edit Flow Tools Reports Window Layout View Help Quick Access

Flow Navigator PROJECT MANAGER - smux

**PROJECT MANAGER**

- Settings
- Add Sources
- Language Templates
- IP Catalog
- IP INTEGRATOR
  - Create Block Design
  - Open Block Design
  - Generate Block Design
- SIMULATION
- RTL ANALYSIS
  - Open Elaborated Design
- SYNTHESIS**
  - Run Synthesis**
  - Open Synthesized Design
- IMPLEMENTATION
  - Run Implementation
  - Open Implemented Design
- PROGRAM AND DEBUG
  - Generate Bitstream
  - Open Hardware Manager

**Sources**

- Design Sources (1)
  - smux (smux.v)
- Constraints
  - constrs\_1
- Simulation Sources (1)
  - sim\_1 (1)

**Synthesis Run Properties**

- synth\_1

**Synthesis Completed**

- Synthesis successfully completed.
- Next
  - Run Implementation
  - Open Synthesized Design**
  - View Reports
  - Don't show this dialog again
- OK Cancel

**Design Runs**

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy
✓ synth_1	constrs_1	synth_design Complete!								1	0	0.0	0	0	2/10/20, 3:56 PM	00:00:34	Vivado Synthesis Defaults (Vivado Synthesis 2019)
▷ impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implement

Tcl Console Messages Log Reports Design Runs

double click

# I/O Pins Assignment (2/4)

3

Remember to save your assignment

1

File Edit Flow Tools Reports Window Layout View Help

SYNTHESIZED DESIGN \* - xc7a35tcbg236-1

Internal VREF

0.6V  
0.675V  
0.75V  
0.9V

Drop I/O banks on voltages or the "NONE" folder to set/unset Internal VREF.

I/O Port Properties

Name: out  
Direction: OUT  
Package pin: U16 [Fixed]  
Site type: IO\_L23N\_T3\_A02\_D18\_14  
Site info: IOB\_X0Y3  
Cell: out\_OBUF\_inst

Name	Direction	Interface	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std	Vcco	Vref	Drive Strength
a	IN			V17	<input checked="" type="checkbox"/>	14	LVCMOS33*	3.300		
b	IN			V16	<input checked="" type="checkbox"/>	14	LVCMOS33*	3.300		
out	OUT			U16	<input checked="" type="checkbox"/>	14	LVCMOS33*	3.300	12	
sel	IN			W16	<input checked="" type="checkbox"/>	14	LVCMOS33*	3.300		

Save Constraints

Select a target file to write new unsaved constraints to. Choosing an existing file will update that file with the new constraints.

**type the constraint file name**

Create a new file

File type: XDC

File name: smux.xdc

File location: <Local to Project>

Select an existing file

<select a target file>

OK Cancel

# I/O Pins Assignment (3/4)

smux - [C:/Users/hp/LD/smux/smux.xpr] - Vivado 2019.2

File Edit Flow Tools Reports Window Layout View Help

Synthesis Out-of-date details

I/O Planning

Flow Navigator

PROJECT MANAGER

- Settings
- Add Sources
- Language Templates
- IP Catalog

IP INTEGRATOR

- Create Block Design
- Open Block Design
- Generate Block Design

SIMULATION

RTL ANALYSIS

- Open Elaborated Design

SYNTHESIS

- Run Synthesis
- Open Synthesized Design
  - Constraints Wizard
  - Edit Timing Constraints
  - Set Up Debug
  - Report Timing Summary
  - Report Clock Networks
  - Report Clock Interaction
  - Report Methodology
  - Report DRC
  - Report Noise
  - Report Utilization

SYNTHESIZED DESIGN - xc7a35tcbg236-1

Sources Netlist Device Constraints

Internal VREF

- 0.6V
- 0.675V
- 0.75V
- 0.9V

Drop I/O banks on voltages or the "NONE" folder to set/unset Internal VREF.

I/O Port Properties

out

Name: out

Direction: OUT

Package pin: U16  Fixed

Site type: IO\_L23N\_T3\_A02\_D18\_14

Site info: IOB\_X0Y3

Cell: out\_OBUF\_inst

General Properties Configure Power

Package Device smux.v test\_smux.v

Confirm Close

OK to close 'Synthesized Design'?

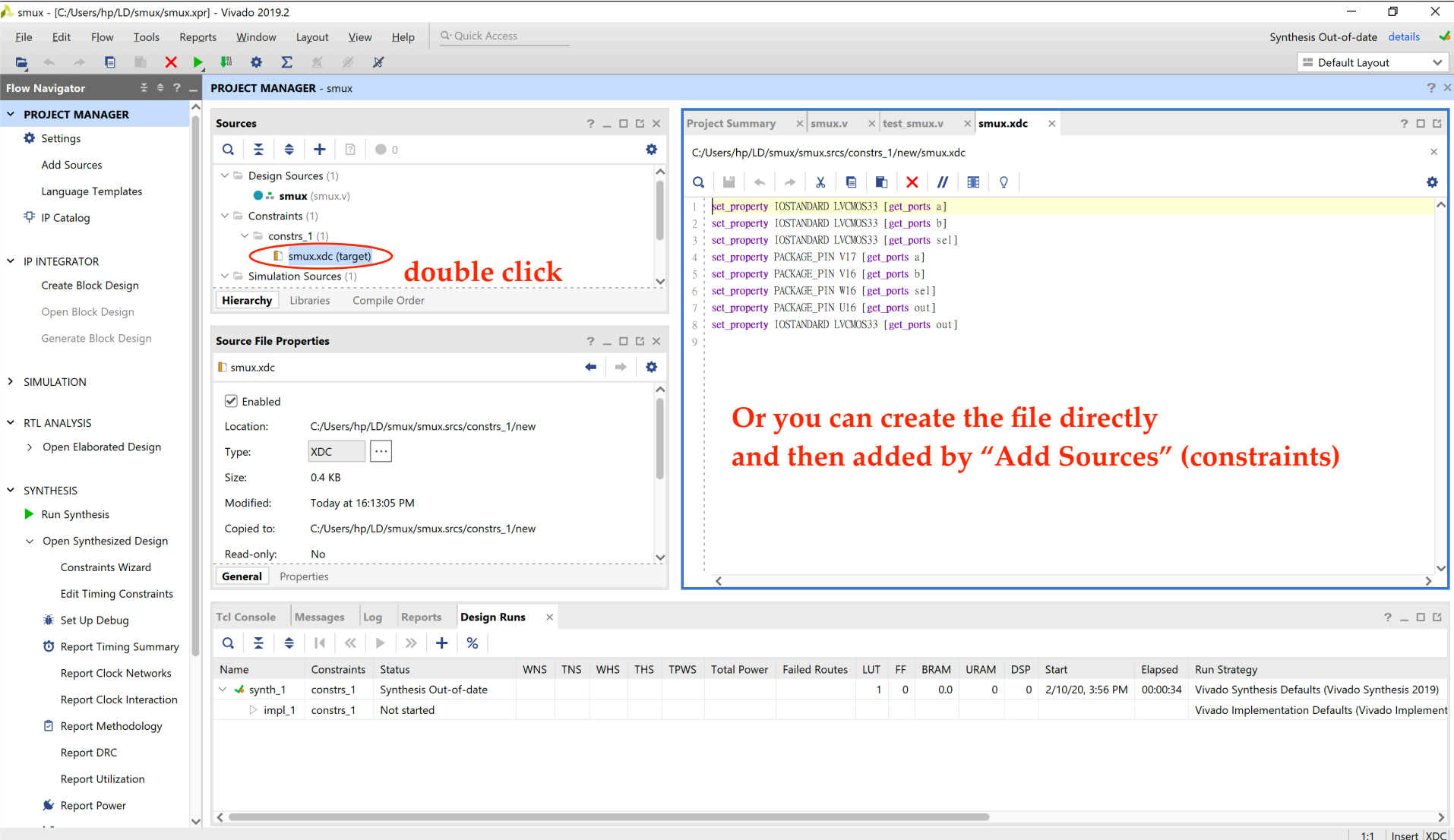
Don't show this dialog again

OK Cancel

Tcl Console Messages Log Reports Design Runs Package Pins I/O Ports

Name	Direction	Interface	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std	Vcco	Vref	Drive Strength	Slew Type	Pull Type	Off-Chip Termination	IN_TERM
a	IN			V17	<input checked="" type="checkbox"/>	14	LVCMOS33*	3.300				NONE	NONE	
b	IN			V16	<input checked="" type="checkbox"/>	14	LVCMOS33*	3.300				NONE	NONE	
out	OUT			U16	<input checked="" type="checkbox"/>	14	LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_50	
sel	IN			W16	<input checked="" type="checkbox"/>	14	LVCMOS33*	3.300				NONE	NONE	

# I/O Pins Assignment (4/4)



The screenshot shows the Vivado 2019.2 interface. The **PROJECT MANAGER** pane on the left shows the project structure with **smux.xdc (target)** circled in red. A red text annotation **double click** points to this file. The **Source File Properties** pane shows the file is enabled and located at `C:/Users/hp/LD/smux/smux.srcs/constrs_1/new`. The **smux.xdc** file is open in the editor, showing the following constraints:

```

1 set_property IOSTANDARD LVCMOS33 [get_ports a]
2 set_property IOSTANDARD LVCMOS33 [get_ports b]
3 set_property IOSTANDARD LVCMOS33 [get_ports sel]
4 set_property PACKAGE_PIN V17 [get_ports a]
5 set_property PACKAGE_PIN V16 [get_ports b]
6 set_property PACKAGE_PIN W16 [get_ports sel]
7 set_property PACKAGE_PIN U16 [get_ports out]
8 set_property IOSTANDARD LVCMOS33 [get_ports out]
9

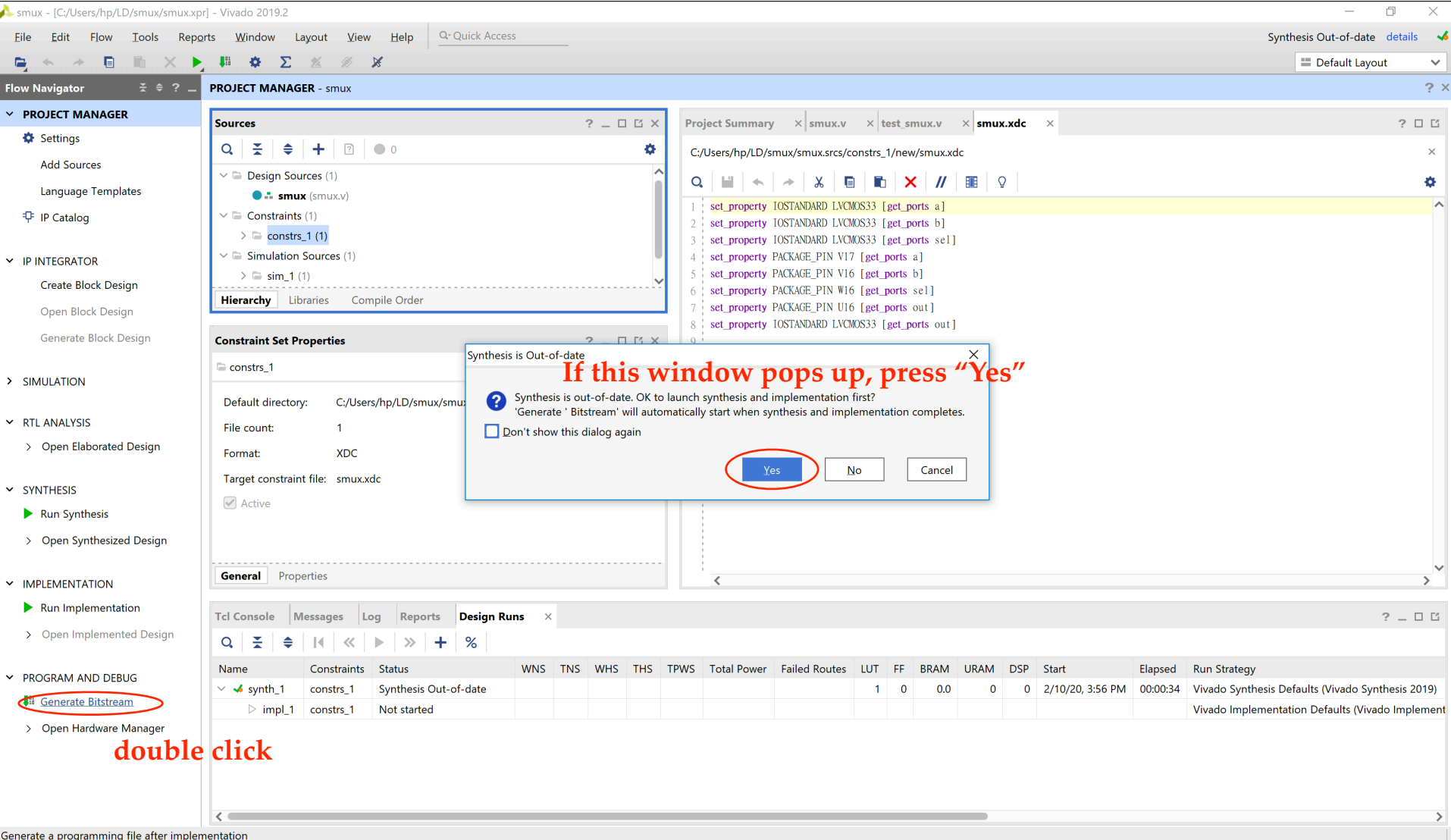
```

A red text annotation **Or you can create the file directly and then added by "Add Sources" (constraints)** is overlaid on the editor window. The **Design Runs** table at the bottom shows the synthesis status:

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy
synth_1	constrs_1	Synthesis Out-of-date								1	0	0.0	0	0	2/10/20, 3:56 PM	00:00:34	Vivado Synthesis Defaults (Vivado Synthesis 2019)
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implement)



# Synthesis and Implementation (1/7)



smux - [C:/Users/hp/LD/smux/smux.xpr] - Vivado 2019.2  
 File Edit Flow Tools Reports Window Layout View Help

**Flow Navigator**  
 PROJECT MANAGER - smux

**Sources**  
 Design Sources (1)  
 smux (smux.v)  
 Constraints (1)  
 constrs\_1 (1)  
 Simulation Sources (1)  
 sim\_1 (1)

**Constraint Set Properties**  
 Default directory: C:/Users/hp/LD/smux/smux...  
 File count: 1  
 Format: XDC  
 Target constraint file: smux.xdc  
 Active

**Project Summary**  
 C:/Users/hp/LD/smux/smux.srcs/constrs\_1/new/smux.xdc  

```

1 set_property IOSTANDARD LVCMOS33 [get_ports a]
2 set_property IOSTANDARD LVCMOS33 [get_ports b]
3 set_property IOSTANDARD LVCMOS33 [get_ports sel]
4 set_property PACKAGE_PIN V17 [get_ports a]
5 set_property PACKAGE_PIN V16 [get_ports b]
6 set_property PACKAGE_PIN W16 [get_ports sel]
7 set_property PACKAGE_PIN U16 [get_ports out]
8 set_property IOSTANDARD LVCMOS33 [get_ports out]

```

**Synthesis is Out-of-date**  
 Synthesis is out-of-date. OK to launch synthesis and implementation first?  
 'Generate' Bitstream' will automatically start when synthesis and implementation completes.  
 Don't show this dialog again  
 Yes No Cancel

**Design Runs**

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy
synth_1	constrs_1	Synthesis Out-of-date								1	0	0.0	0	0	2/10/20, 3:56 PM	00:00:34	Vivado Synthesis Defaults (Vivado Synthesis 2019)
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implement)

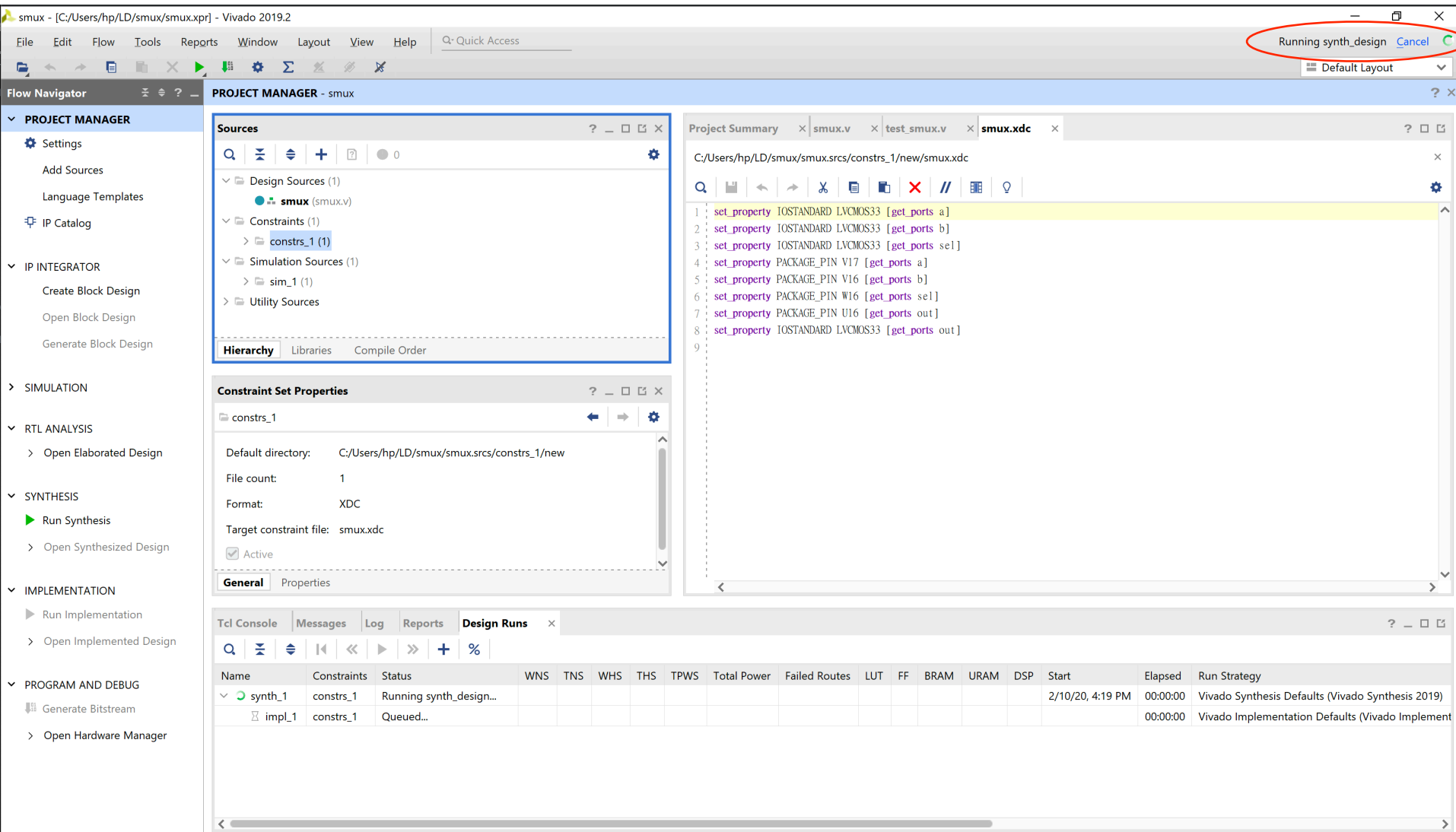
# Generate Bitstream

**double click**

Generate a programming file after implementation

# Synthesis and Implementation (2/7)

implementation progress information



smux - [C:/Users/hp/LD/smux/smux.xpr] - Vivado 2019.2

File Edit Flow Tools Reports Window Layout View Help

Running synth\_design Cancel

Default Layout

Flow Navigator

PROJECT MANAGER - smux

Sources

- Design Sources (1)
  - smux (smux.v)
- Constraints (1)
  - constrs\_1 (1)
- Simulation Sources (1)
  - sim\_1 (1)
- Utility Sources

Hierarchy Libraries Compile Order

Constraint Set Properties

constrs\_1

Default directory: C:/Users/hp/LD/smux/smux.srscs/constrs\_1/new

File count: 1

Format: XDC

Target constraint file: smux.xdc

Active

General Properties

Project Summary | smux.v | test\_smux.v | smux.xdc

C:/Users/hp/LD/smux/smux.srscs/constrs\_1/new/smux.xdc

```

1 ; set_property IOSTANDARD LVCMOS33 [get_ports a]
2 ; set_property IOSTANDARD LVCMOS33 [get_ports b]
3 ; set_property IOSTANDARD LVCMOS33 [get_ports sel]
4 ; set_property PACKAGE_PIN V17 [get_ports a]
5 ; set_property PACKAGE_PIN V16 [get_ports b]
6 ; set_property PACKAGE_PIN W16 [get_ports sel]
7 ; set_property PACKAGE_PIN U16 [get_ports out]
8 ; set_property IOSTANDARD LVCMOS33 [get_ports out]
9
    
```

Tcl Console Messages Log Reports Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy
synth_1	constrs_1	Running synth_design...													2/10/20, 4:19 PM	00:00:00	Vivado Synthesis Defaults (Vivado Synthesis 2019)
impl_1	constrs_1	Queued...														00:00:00	Vivado Implementation Defaults (Vivado Implement)

# Synthesis and Implementation (3/7)

smux - [C:/Users/hp/LD/smux/smux.xpr] - Vivado 2019.2

File Edit Flow Tools Reports Window Layout View Help Q- Quick Access

**1** **Connect and power on the FPGA board**

write\_bitstream Complete

Default Layout

Flow Navigator PROJECT MANAGER - smux

PROJECT MANAGER

- Settings
- Add Sources
- Language Templates
- IP Catalog
- IP INTEGRATOR
  - Create Block Design
  - Open Block Design
  - Generate Block Design
- SIMULATION
- RTL ANALYSIS
  - Open Elaborated Design
- SYNTHESIS
  - Run Synthesis
  - Open Synthesized Design
- IMPLEMENTATION
  - Run Implementation
  - Open Implemented Design
- PROGRAM AND DEBUG
  - Generate Bitstream
  - Open Hardware Manager

Sources

- Design Sources (1)
  - smux (smux.v)
- Constraints (1)
  - constrs\_1 (1)
- Simulation Sources (1)
  - sim\_1 (1)
- Utility Sources

Hierarchy Libraries Compile Order

Constraint Set Properties

constrs\_1

Default directory: C:/Users/hp/LD/smux/smux.srcs/constrs\_1/new

File count: 1

Format: XDC

Target constraint file: smux.xdc

Active

General Properties

Project Summary x smux.v x test\_smux.v x smux.xdc

C:/Users/hp/LD/smux/smux.srcs/constrs\_1/new/smux.xdc

```

1 ; set_property IOSTANDARD LVCMOS33 [get_ports a]
2 ; set_property IOSTANDARD LVCMOS33 [get_ports b]
3 ; set_property IOSTANDARD LVCMOS33 [get_ports sel]
4 ; set_property PACKAGE_PIN V17 [get_ports a]
5 ; set_property PACKAGE_PIN V16 [get_ports b]

```

Bitstream Generation Completed

Bitstream Generation successfully completed.

Next

- Open Implemented Design
- View Reports
- Open Hardware Manager
- Generate Memory Configuration File
- Don't show this dialog again

OK Cancel

Tcl Console Messages Log Reports Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy
synth_1	constrs_1	synth_design Complete!								1	0	0.0	0	0	2/10/20, 4:19 PM	00:00:44	Vivado Synthesis Defaults (Vivado Synthesis 2
impl_1	constrs_1	write_bitstream Complete!	NA	NA	NA	NA	NA	1.103	0	1	0	0.0	0	0	2/10/20, 4:20 PM	00:01:09	Vivado Implementation Defaults (Vivado Impl

Constraint Set: constrs\_1

After synthesis and implementation

# Synthesis and Implementation (4/7)

smux - [C:/Users/hp/LD/smux/smux.xpr] - Vivado 2019.2

File Edit Flow Tools Reports Window Layout View Help Quick Access

Dashboard

write\_bitstream Complete

Default Layout

Flow Navigator

**HARDWARE MANAGER - unconnected**

No hardware target is open. **Open target**

Hardware

- Auto Connect
- Recent Targets
- Available Targets on Server
- Open New Target...

Constraint Set Properties

constrs\_1

Default directory: C:/Users/hp/LD/smux/smux.srscs/o

File count: 1

Format: XDC

Target constraint file: smux.xdc

Active

General Properties

smux.v x test\_smux.v x smux.xdc x

C:/Users/hp/LD/smux/smux.srscs/sources\_1/new/smux.v

```

1 timescale 1ns / 1ps
2 ///////////////////////////////////////////////////
3 //Company:
4 //Engineer:
5 //
6 //Create Date: 02/10/2020 01:46:53 PM
7 //Design Name:
8 //Module Name: smux
9 //Project Name:
10 //Target Devices:
11 //Tool Versions:
12 //Description:
13 //
14 //Dependencies:
15 //
16 //Revision:
17 //Revision 0.01 - File Created
18 //Additional Comments:
19 //
20 ///////////////////////////////////////////////////
21

```

Tcl Console

```

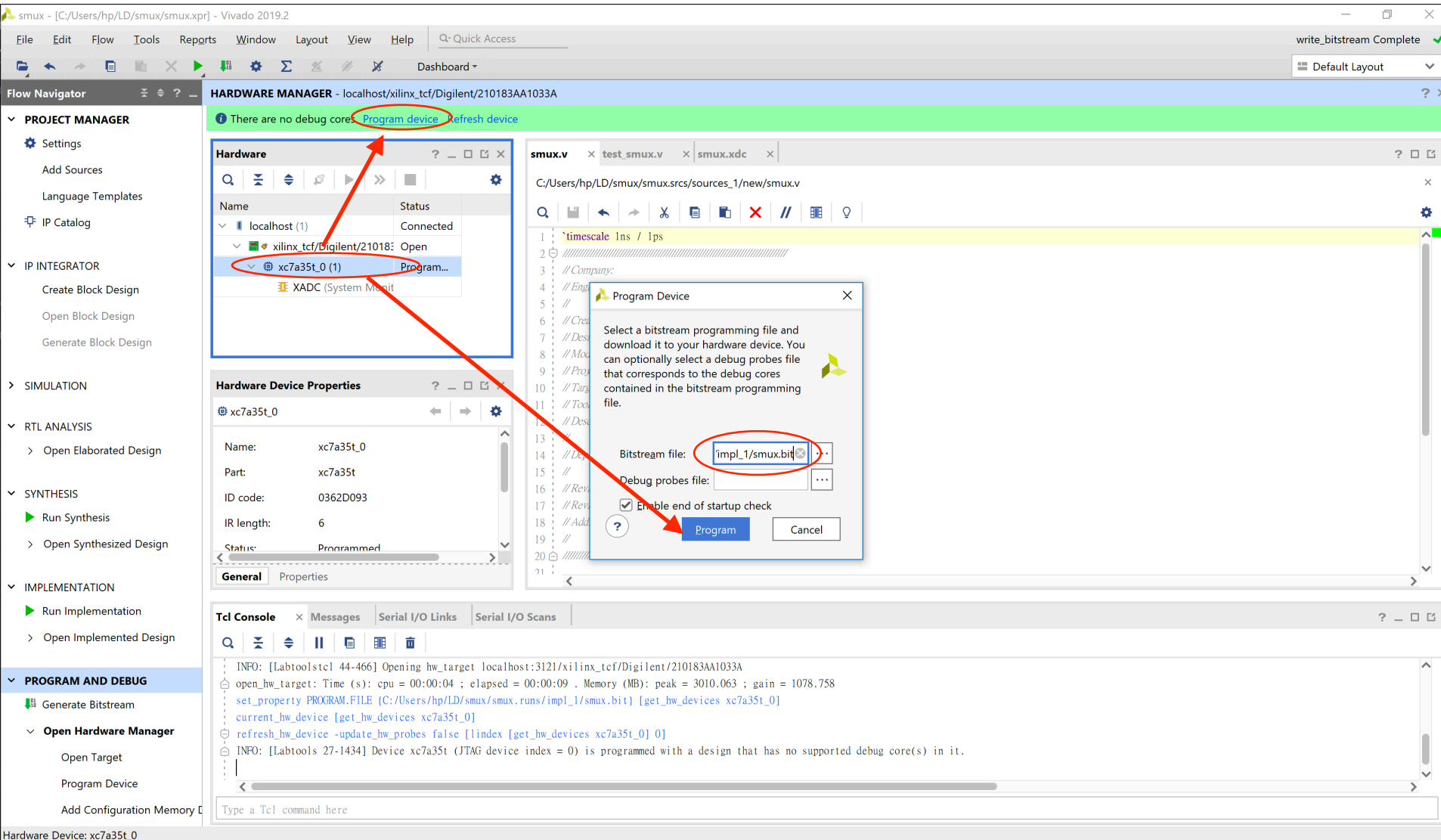
launch_runs impl_1 -to_step write_bitstream
[Mon Feb 10 16:19:40 2020] Launched synth_1...
Run output will be captured here: C:/Users/hp/LD/smux/smux.runs/synth_1/runme.log
[Mon Feb 10 16:19:40 2020] Launched impl_1...
Run output will be captured here: C:/Users/hp/LD/smux/smux.runs/impl_1/runme.log
open_hw_manager

```

Type a Tcl command here

Automatically connect to local hardware target

# Synthesis and Implementation (5/7)



The screenshot shows the Vivado 2019.2 interface with the following components:

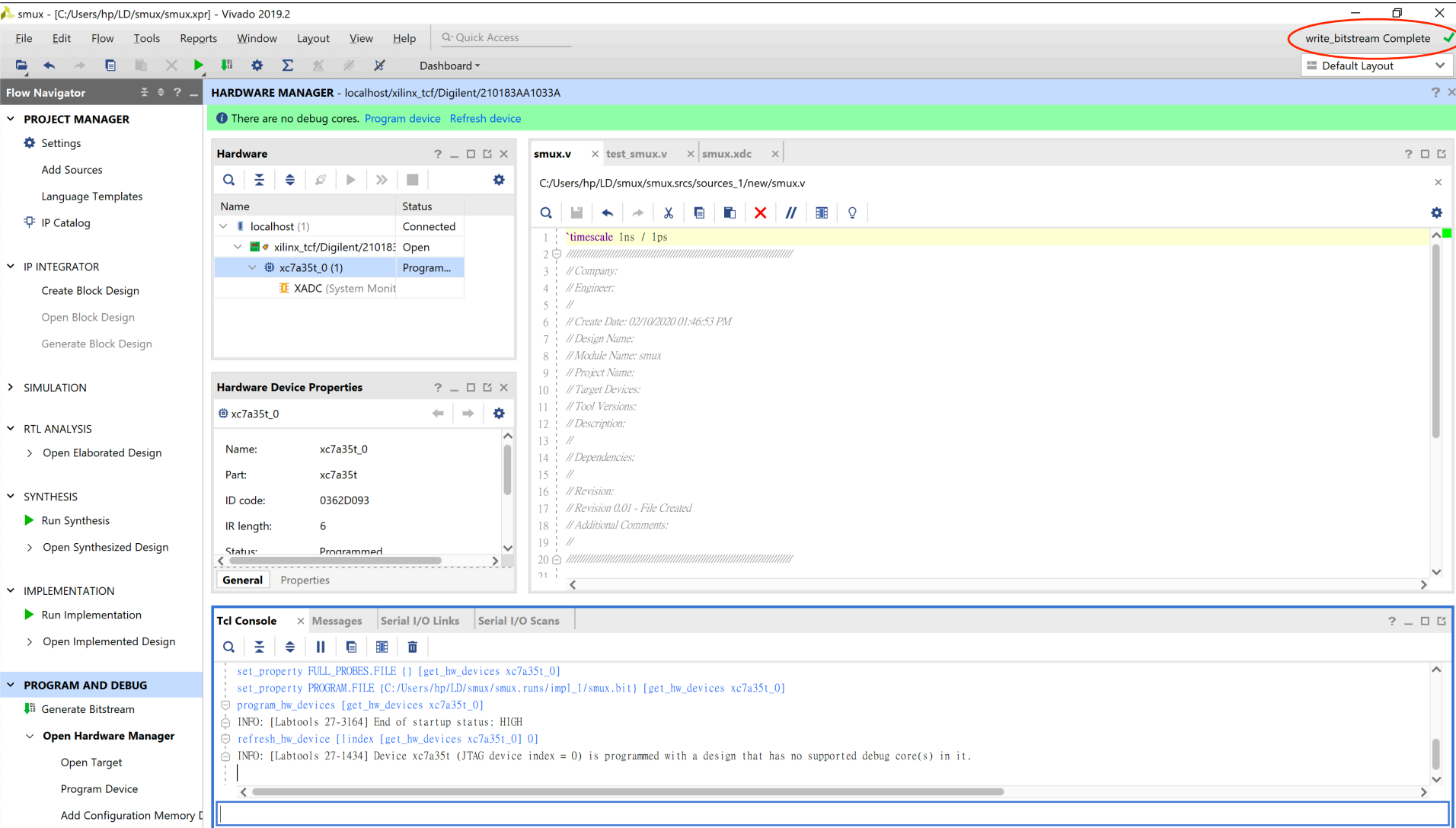
- Flow Navigator:** Shows the project structure with "PROGRAM AND DEBUG" selected.
- HARDWARE MANAGER:** Displays a table of hardware components:
 

Name	Status
localhost (1)	Connected
xilinx_tcf/Digilent/210183	Open
xc7a35t_0 (1)	Program...
- Hardware Device Properties:** Shows details for xc7a35t\_0:
  - Name: xc7a35t\_0
  - Part: xc7a35t
  - ID code: 0362D093
  - IR length: 6
  - Status: Programmed
- Program Device Dialog:** A modal window titled "Program Device" with the following fields:
  - Bitstream file: impl\_1/smux.bit (circled in red)
  - Debug probes file: (empty)
  - Enable end of startup check:
  - Buttons: Program, Cancel
- Tcl Console:** Shows the following output:
 

```

INFO: [Labtoolstc1 44-466] Opening hw_target localhost:3121/xilinx_tcf/Digilent/210183AA1033A
open_hw_target: Time (s): cpu = 00:00:04 ; elapsed = 00:00:09 . Memory (MB): peak = 3010.063 ; gain = 1078.758
set_property PROGRAM.FILE {C:/Users/hp/LD/smux/smux.srsrcs/sources_1/new/smux.v} [get_hw_devices xc7a35t_0]
current_hw_device [get_hw_devices xc7a35t_0]
refresh_hw_device -update_hw_probes false [lindex [get_hw_devices xc7a35t_0] 0]
INFO: [Labtools 27-1434] Device xc7a35t (JTAG device index = 0) is programmed with a design that has no supported debug core(s) in it.
      
```

# Synthesis and Implementation (6/7)



smux - [C:/Users/hp/LD/smux/smux.xpr] - Vivado 2019.2

File Edit Flow Tools Reports Window Layout View Help Quick Access

Dashboard

**Flow Navigator**

- PROJECT MANAGER
  - Settings
  - Add Sources
  - Language Templates
  - IP Catalog
- IP INTEGRATOR
  - Create Block Design
  - Open Block Design
  - Generate Block Design
- SIMULATION
- RTL ANALYSIS
  - Open Elaborated Design
- SYNTHESIS
  - Run Synthesis
  - Open Synthesized Design
- IMPLEMENTATION
  - Run Implementation
  - Open Implemented Design
- PROGRAM AND DEBUG**
  - Generate Bitstream
  - Open Hardware Manager
    - Open Target
    - Program Device
    - Add Configuration Memory

**HARDWARE MANAGER** - localhost/xilinx\_tcf/Digilent/210183AA1033A

There are no debug cores. Program device Refresh device

**Hardware**

Name	Status
localhost (1)	Connected
xilinx_tcf/Digilent/210183AA1033A	Open
xc7a35t_0 (1)	Program...
XADC (System Monit	

**Hardware Device Properties**

Name:	xc7a35t_0
Part:	xc7a35t
ID code:	0362D093
IR length:	6
Status:	Programmed

**smux.v**

```

1 timescale 1ns / 1ps
2 //////////////////////////////////////////////////
3 // Company:
4 // Engineer:
5 //
6 // Create Date: 02/10/2020 01:46:53 PM
7 // Design Name:
8 // Module Name: smux
9 // Project Name:
10 // Target Devices:
11 // Tool Versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //////////////////////////////////////////////////
21
  
```

**Tcl Console**

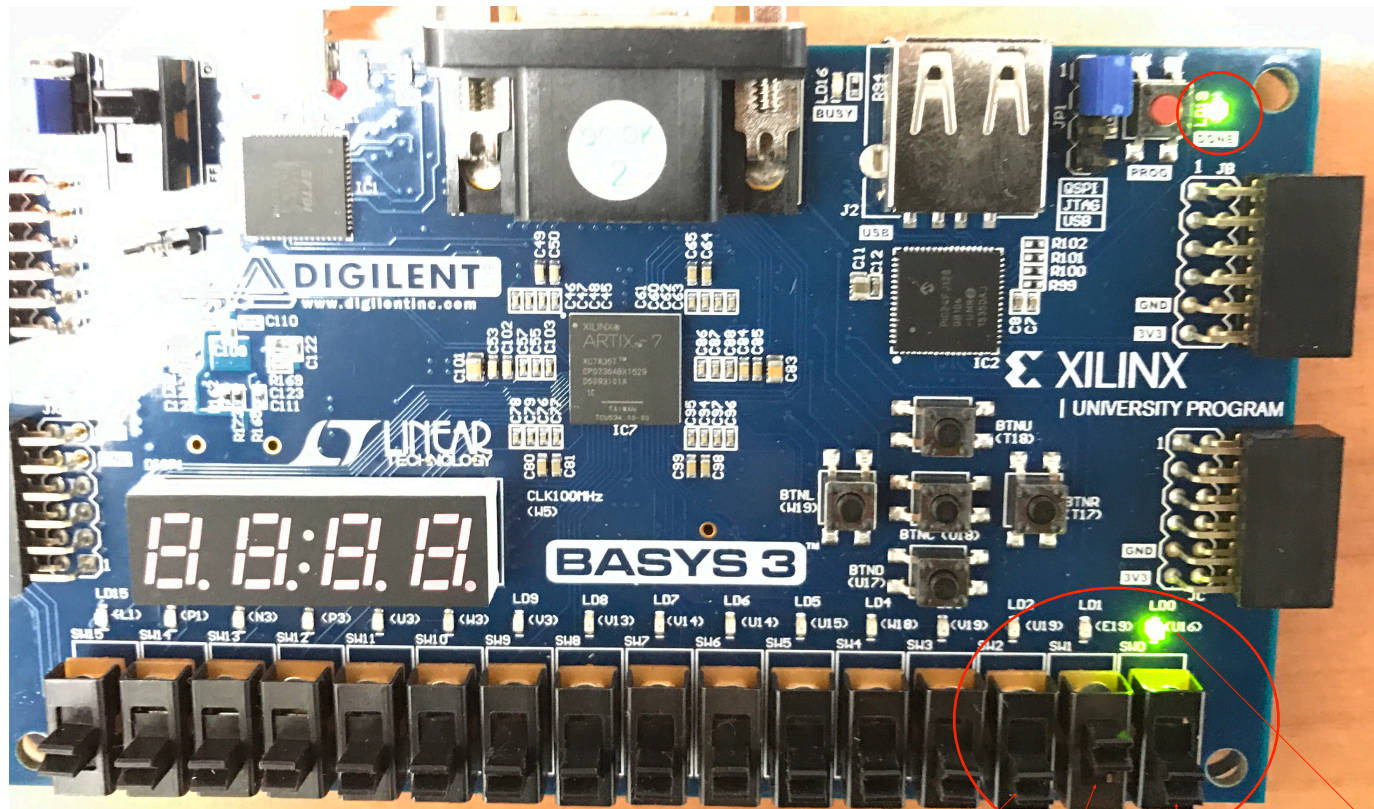
```

set_property FULL_PROBES.FILE {} [get_hw_devices xc7a35t_0]
set_property PROGRAM.FILE [C:/Users/hp/LD/smux/smux.runs/impl_1/smux.bit] [get_hw_devices xc7a35t_0]
program_hw_devices [get_hw_devices xc7a35t_0]
INFO: [Labtools 27-3164] End of startup status: HIGH
refresh_hw_device [lindex [get_hw_devices xc7a35t_0] 0]
INFO: [Labtools 27-1434] Device xc7a35t (JTAG device index = 0) is programmed with a design that has no supported debug core(s) in it.
  
```

write\_bitstream Complete ✓

# Synthesis and Implementation (7/7)

Program Finished



sel=0, b=1, a=0 ==> out=1

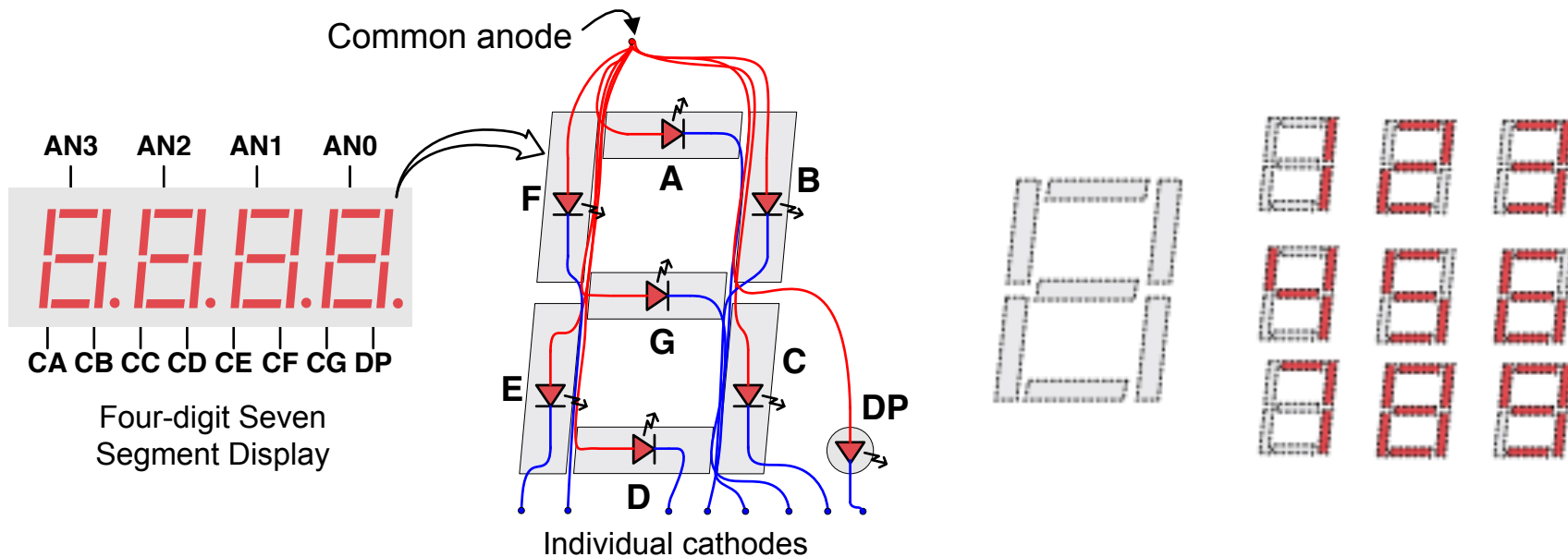
# Some Notes

- Sometimes, the database of the design will be corrupted, and any changes will not take effect or your board behaves weird.
  - Open a new project with fresh source files.
- Look into the 'Errors' or 'Warnings' windows to debug your design.
- If you finish your lab at dorm and want to bring it to the lab for demo
  - DO NOT copy the entire directory to the lab and use the same directory for demo
    - Just copying the .v and .xdc files to the lab is sufficient.
    - Use 'New Project' in the lab and open the existing source files to re-implement your design for demo



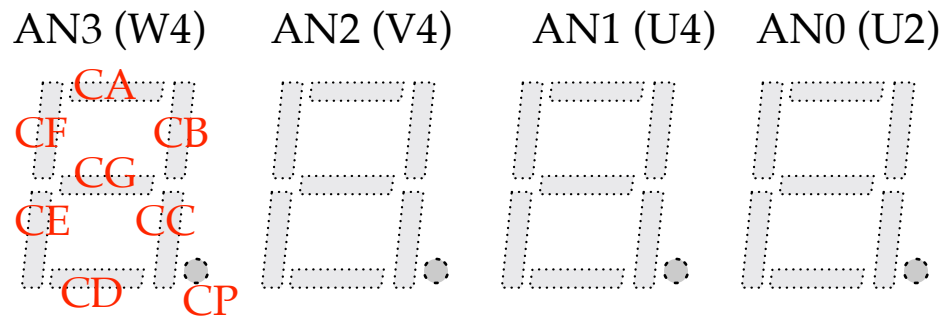
# 7-Segment Display (1/2)

- The anodes of segments forming each digit on all four displays are connected to the same FPGA pin (AN3, AN2, AN1, AN0) (common anode)



## 7-Segment Display (2/2)

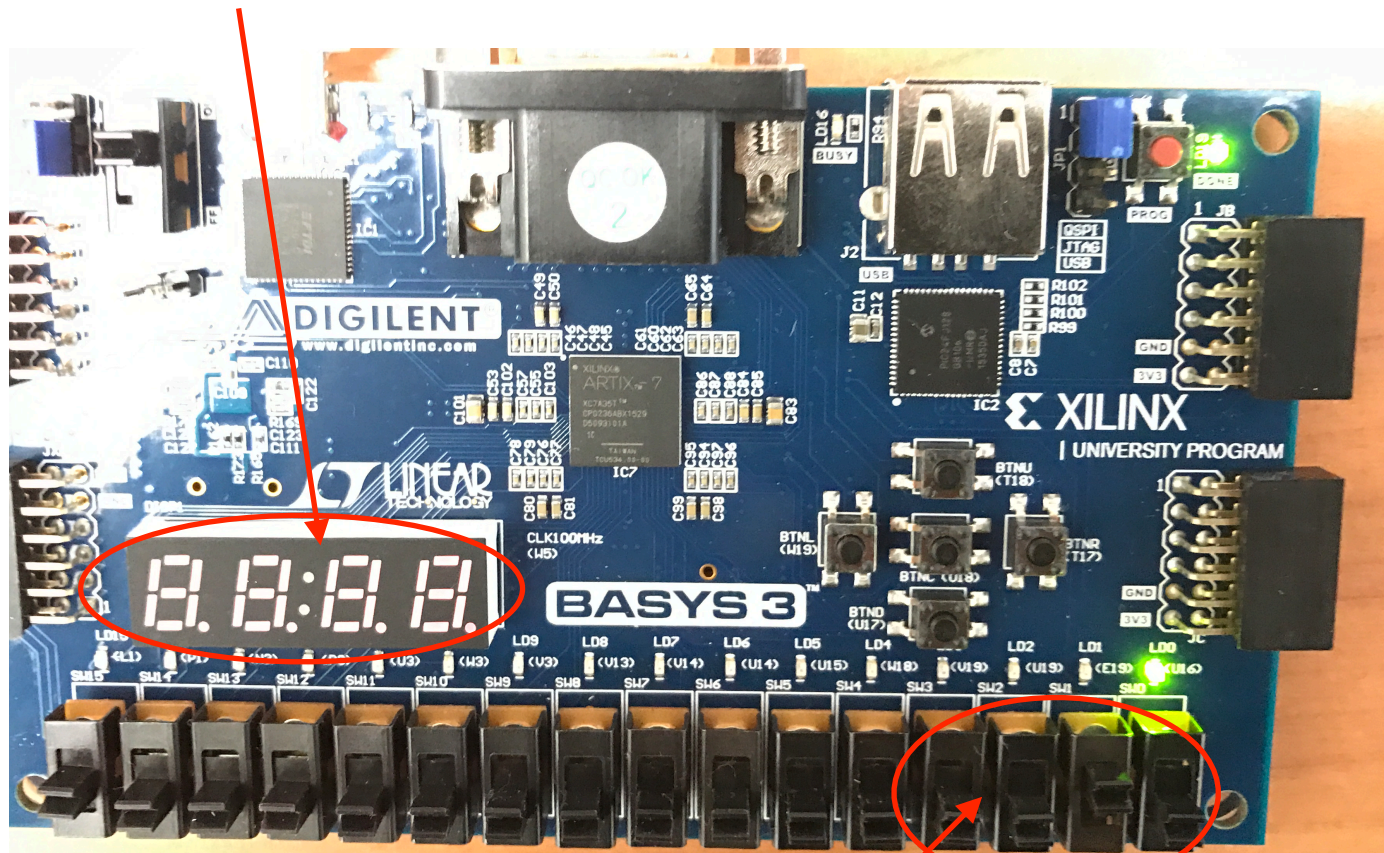
- 8 pins to control each 7-segment display
  - Including the point
- 4 pins (W4, V4, U4, U2) to choose which 7-seg to display
- Device is low activated



Symbol	CA	CB	CC	CD	CE	CF	CG	CP
FPGA Pin	W7	W6	U8	V8	U5	V5	U7	V7

# Example

All 4 digits of 7-Seg Display show same number (BCD number output)

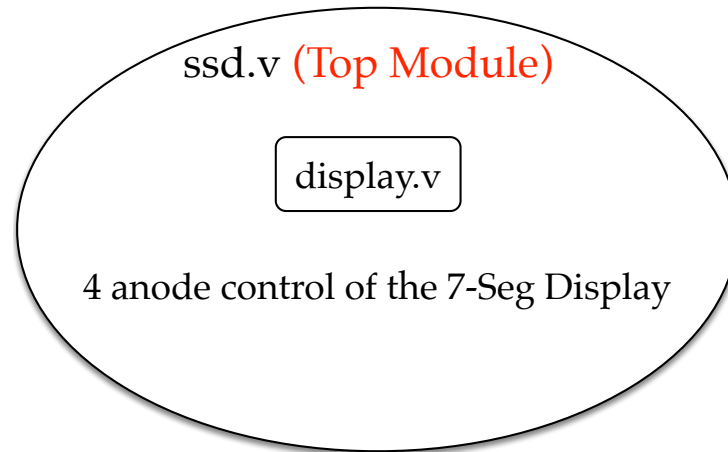


MSB

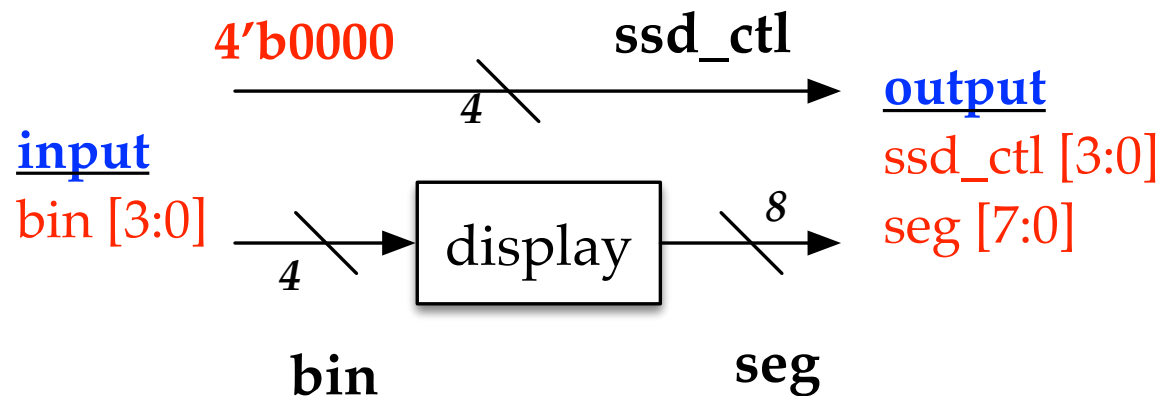
binary input: bin[3:0]

# Block Diagram for 7-Seg Display

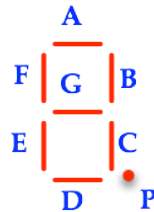
## System Hierarchy



## Block Diagram



# A BCD to Seven-Segment Display Decoder



```
// define segment codes
`define SS_0 8'b00000011
`define SS_1 8'b10011111
`define SS_2 8'b00100101
`define SS_3 8'b00001101
`define SS_4 8'b10011001
`define SS_5 8'b01001001
`define SS_6 8'b01000001
`define SS_7 8'b00011111
`define SS_8 8'b00000001
`define SS_9 8'b00001001
```

```
module display(segs, bin);
output [7:0] segs;
input [3:0] bin;
reg [7:0] segs;

always @*
  case (bin)
    4'd0: segs = `SS_0;
    4'd1: segs = `SS_1;
    4'd2: segs = `SS_2;
    4'd3: segs = `SS_3;
    4'd4: segs = `SS_4;
    4'd5: segs = `SS_5;
    4'd6: segs = `SS_6;
    4'd7: segs = `SS_7;
    4'd8: segs = `SS_8;
    4'd9: segs = `SS_9;
    default: segs = 8'b00000000;
  endcase
endmodule
```

# Top Module (ssd.v)

```
module ssd(seg, bin, ssd_ctl);  
output [3:0] ssd_ctl;  
output [7:0] seg;  
input [3:0] bin;  
  
display U0(.segs(seg),.bin(bin));  
  
assign ssd_ctl = 4'b0000;  
  
endmodule
```

# ssd.xdc (1 / 2)

# Four anode control signals

```
set_property PACKAGE_PIN W4 [get_ports {ssd_ctl[3]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {ssd_ctl[3]}]
set_property PACKAGE_PIN V4 [get_ports {ssd_ctl[2]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {ssd_ctl[2]}]
set_property PACKAGE_PIN U4 [get_ports {ssd_ctl[1]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {ssd_ctl[1]}]
set_property PACKAGE_PIN U2 [get_ports {ssd_ctl[0]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {ssd_ctl[0]}]
```

#8 common segment controls

```
set_property PACKAGE_PIN W7 [get_ports {seg[7]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {seg[7]}]
set_property PACKAGE_PIN W6 [get_ports {seg[6]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {seg[6]}]
set_property PACKAGE_PIN U8 [get_ports {seg[5]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {seg[5]}]
set_property PACKAGE_PIN V8 [get_ports {seg[4]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {seg[4]}]
```

## ssd.xdc (2/2)

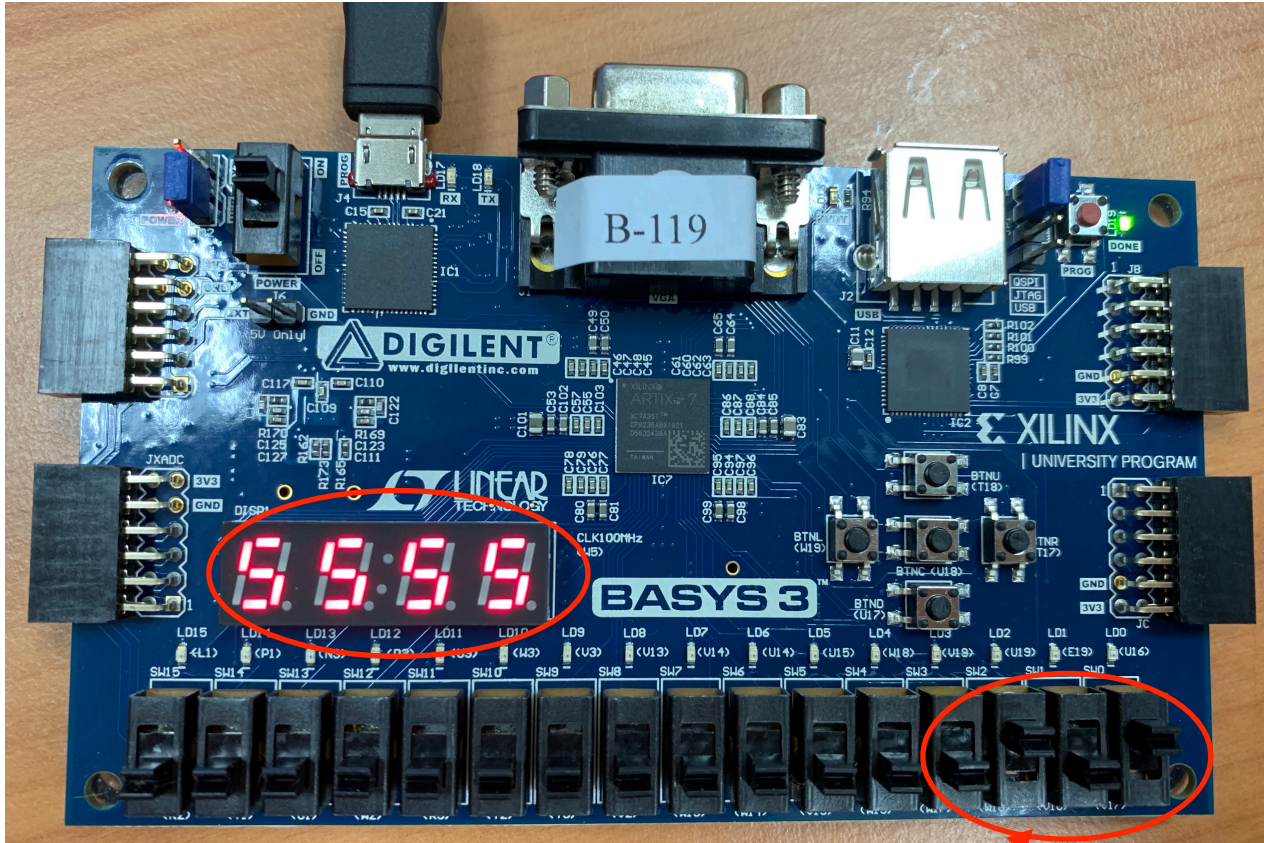
```
set_property PACKAGE_PIN U5 [get_ports {seg[3]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {seg[3]}]
set_property PACKAGE_PIN V5 [get_ports {seg[2]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {seg[2]}]
set_property PACKAGE_PIN U7 [get_ports {seg[1]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {seg[1]}]
set_property PACKAGE_PIN V7 [get_ports {seg[0]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {seg[0]}]
```

### #4-bit binary input

```
set_property PACKAGE_PIN W17 [get_ports {bin[3]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {bin[3]}]
set_property PACKAGE_PIN W16 [get_ports {bin[2]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {bin[2]}]
set_property PACKAGE_PIN V16 [get_ports {bin[1]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {bin[1]}]
set_property PACKAGE_PIN V17 [get_ports {bin[0]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {bin[0]}]
```



# Example



binary input: 0101