邏輯設計實驗 preLab5

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1 Construct a 30-second down counter with pause function. When the counter goes to 0, all the LEDs will be lighted up. You can use one push button for reset and one other for pause/start function.

1.1 Write the spec (inputs, outputs, and function table) of the design.

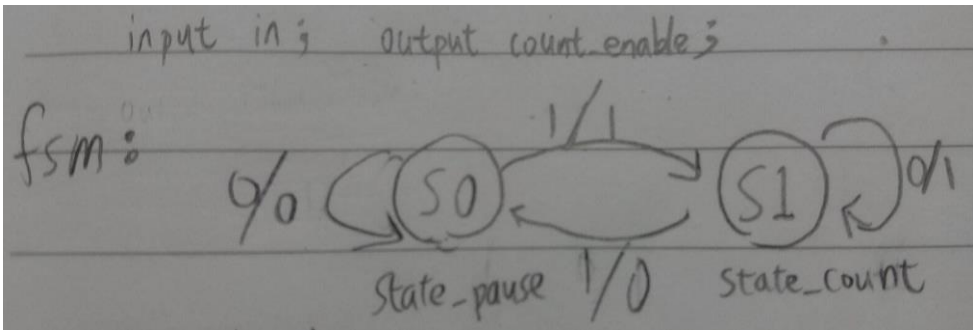
1.fsm：

input rst,clk,in;　//in 即是我的按鍵，控制 pause/start

output reg state;

reg next_state;

output reg count_enable;



2.count_down：

input clk,rst;

input en;

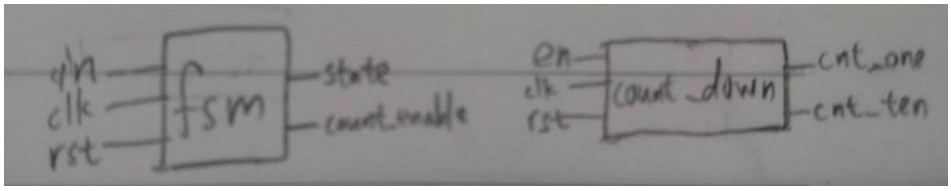
output reg [3:0]cnt_one;

reg [3:0]cnt_one_tmp;

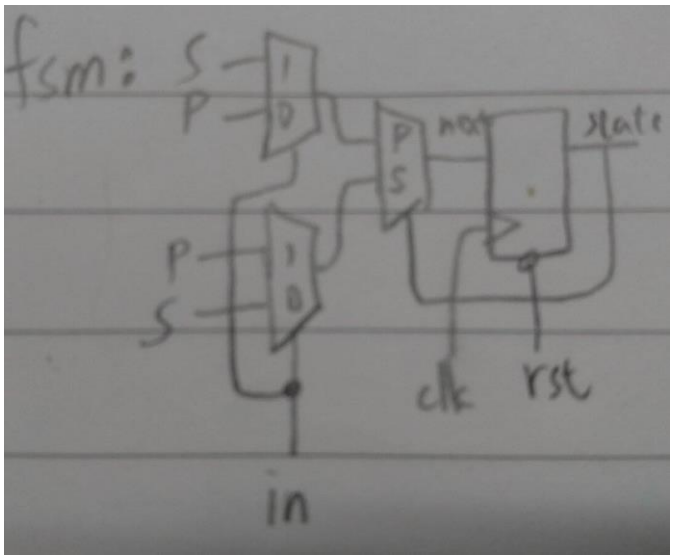
output reg [3:0]cnt_ten;

reg [3:0]cnt_ten_tmp;

1.2 Draw the related block/logic diagram.



1.3 Use a FSM to implement the function of pause/start function. Use one LED to represent current state.



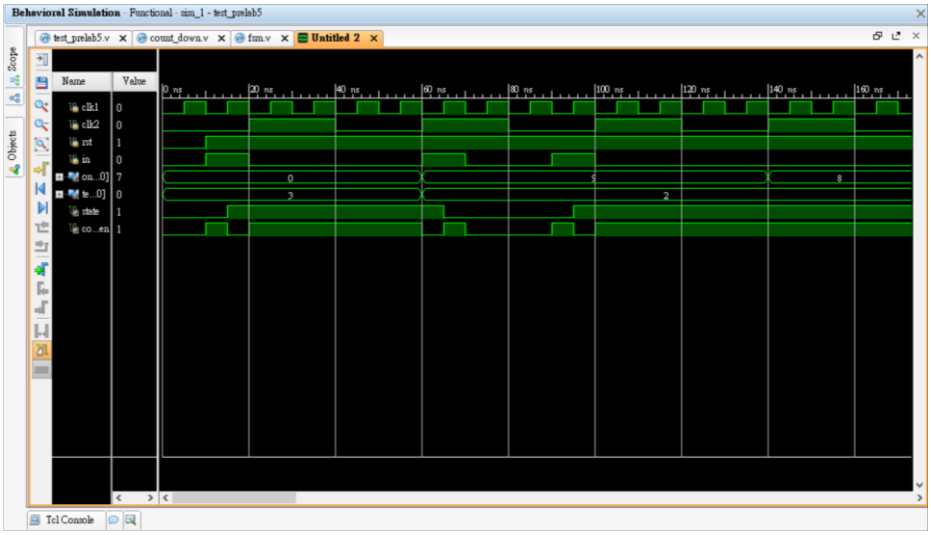
1.4 Use Verilog to implement 1.3 and verify the design with simulation results. Draw the logic diagram

Result

在此 clk1 是接到 fsm 的；clk2 是接到 count_down 的

fsm T0(.in(in),.clk(clk1),.rst(rst),.state(state),.count_enable(count_en));

count_down T1(.clk(clk2),.rst(rst),.cnt_one(one),.cnt_ten(ten),.en(count_en));



一開始 rst=0;clk1=0;in=0;clk2=0;→state=0(表示 pause)，當第一個 in=1 出現時，state 在 clk1 從 0→1 時值變成 1(start)，因此數字開始往下數。當第二個 in=1 出現時，state 在 clk1 從 0→1 時值變成 0(pause)，也跟著暫停往下數。