邏輯設計實驗preLab5

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**1 Construct a 30-second down counter with pause function. When the counter goes to 0, all the LEDs will be lighted up. You can use one push button for reset and one other for pause/start function.**

* 1. **Write the spec (inputs, outputs, and function table) of the design.**

1.fsm：

input rst,clk,in; //in即是我的按鍵，控制pause/start

output reg state;

reg next\_state;

 output reg count\_enable;

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2.count\_down：

 input clk,rst;

 input en;

 output reg [3:0]cnt\_one;

 reg [3:0]cnt\_one\_tmp;

 output reg [3:0]cnt\_ten;

 reg [3:0]cnt\_ten\_tmp;

* 1. **Draw the related block/logic diagram.**

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* 1. **Use a FSM to implement the function of pause/start function. Use one LED to represent current state.**

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**1.4 Use Verilog to implement 1.3 and verify the design with simulation results. Draw the logic diagram**

Result

在此clk1是接到fsm的；clk2是接到count\_down的

 fsm T0(.in(in),.clk(clk1),.rst(rst),.state(state),.count\_enable(count\_en));

 count\_down T1(.clk(clk2),.rst(rst),.cnt\_one(one),.cnt\_ten(ten),.en(count\_en));



一開始rst=0;clk1=0;in=0;clk2=0;🡪state=0(表示pause)，當第一個in=1出現時，state在clk1從0🡪1時值變成1(start)，因此數字開始往下數。當第二個in=1出現時，state在clk1從0🡪1時值變成0(pause)，也跟著暫停往下數。