邏輯設計實驗 preLab4

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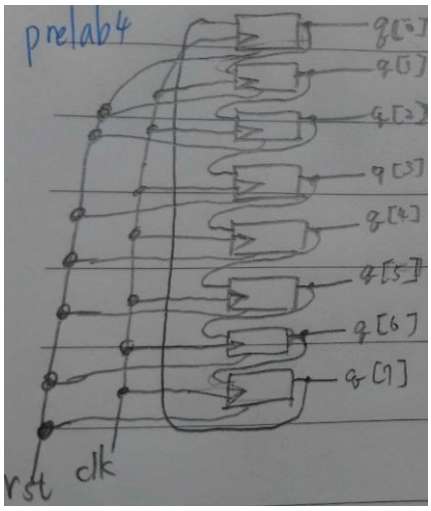
1 Cascade eight DFFs together as a shift register. Connect the output of the last DFF to the input of the first DFF as a ringer counter. Let the initial value of DFF output after reset be 01010101. Construct the Verilog RTL representation for the logics with verification.

1.1 Draw the logic diagram



1.2 Construct Verilog RTL representation for the logics with verification.

```
output [7:0]q;
input rst,clk;
reg [7:0]q;
always@(posedge clk or negedge rst) //此功能為 shifter，每次移一個 bit
    if(~rst) q<=8'b01010101;
    else begin
    q[0]<=q[7];
    q[1]<=q[0];
    q[2]<=q[1];
    q[3]<=q[2];
    q[4]<=q[3];
    q[5]<=q[4];
    q[6]<=q[5];
    q[7]<=q[6];
    end
```

Result

q 每次往右移 1 個 bit，因此從初始值 01010101→10101010→10101010→…