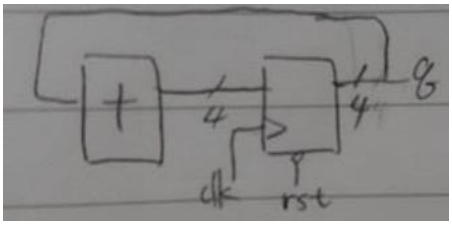
邏輯設計實驗 preLab3

105060012 張育菘

1 Consider a 4-bit synchronous binary up counter.

1.1 Draw the logic diagram



1.2 Construct Verilog RTL representation for the logics with verification.

```
input rst, clk;
output reg [3:0]q;    //q 為一 4-bit 的數
always@(posedge clk or negedge rst)    //clk=1 時加法&讀值
   if(~rst)         //rst = 0 時 reset
      q<=4'b0000;
   else
      q<=q+4'd1;
```