邏輯設計實驗preLab3

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**1 Consider a 4-bit synchronous binary up counter.**

* 1. **Draw the logic diagram**



**1.2 Construct Verilog RTL representation for the logics with verification.**

 input rst, clk;

 output reg [3:0]q; //q為一4-bit的數

 always@(posedge clk or negedge rst) //clk=1時加法&讀值

 if(~rst) //rst = 0時reset

 q<=4'b0000;

 else

 q<=q+4'd1;

