邏輯設計實驗Lab1結報

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**1. Design and implement a full adder. (s+cout=x+y+cin)**

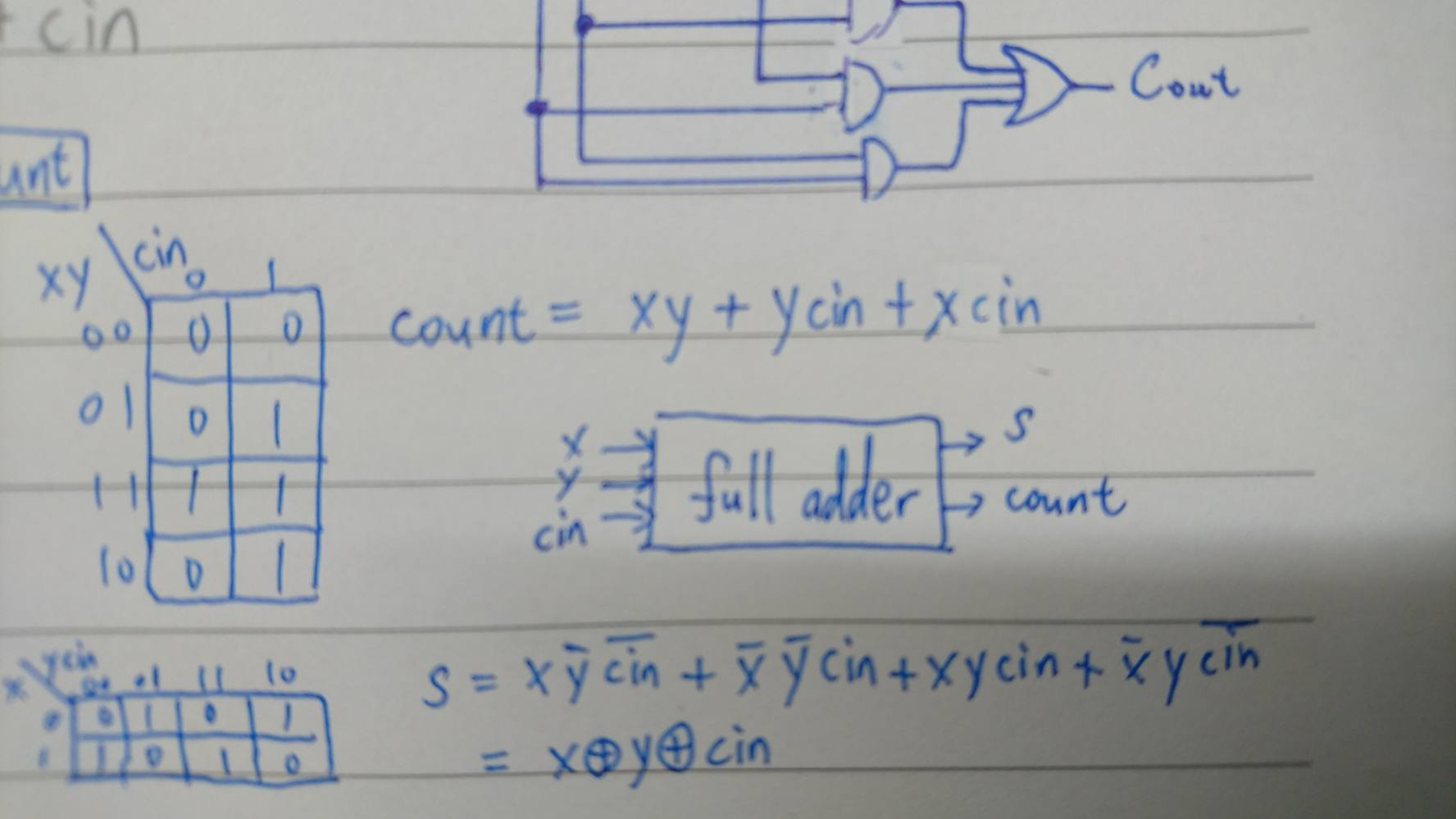
* 1. **Write the logic equation.**
  2. **Draw the related logic diagram.**
  3. **Verilog RTL representation with verification.**

Design Specification

input : x, y, cin;

output : count, s;

block diagram :



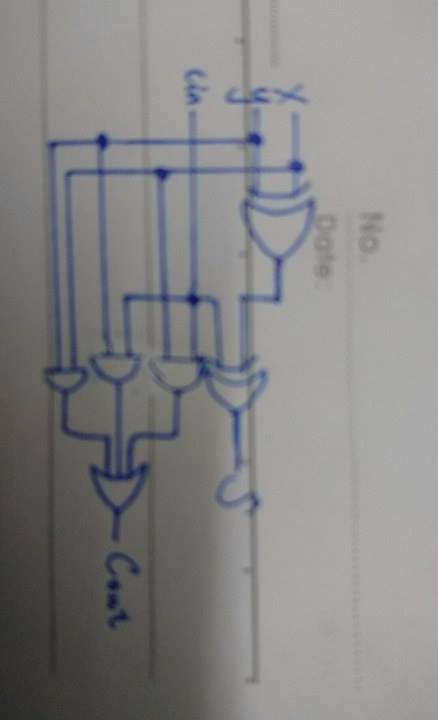
Design Implementation

Logic function :

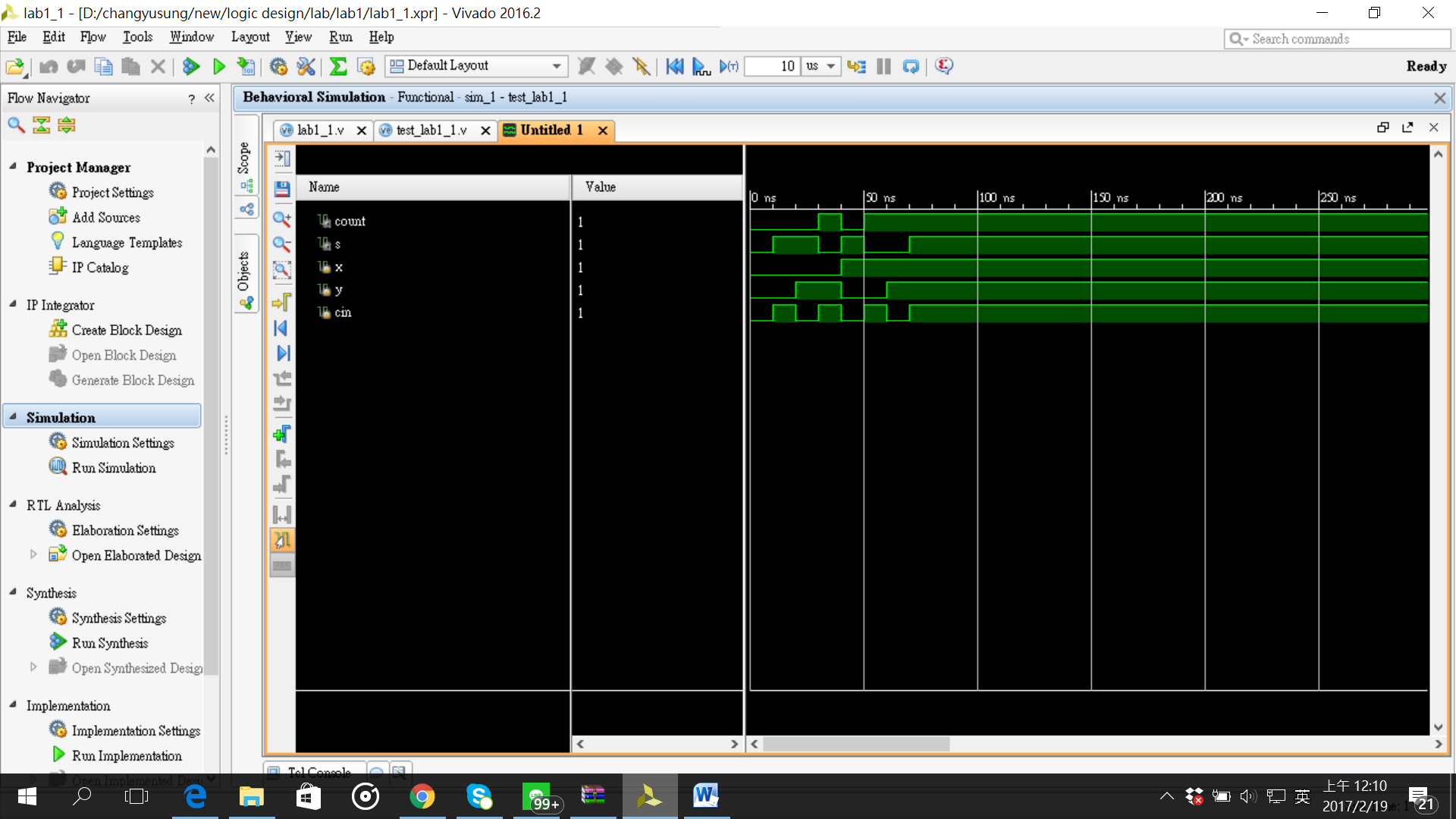
s = x^y^cin

count = (x&y)|(x&cin)|(y&cin)

Logic diagram :



Result :



Discussion

1. (x&(~y)&(~cin))| ((~x)&(~y)&cin)|( x&y&cin)|( (~x)&y&(~cin))可以簡化成x^y^cin

**2. Design a single digit decimal adder with input A(a3a2a1a0), B(b3b2b1b0), Cin(ci), and output S(s3s2s1s0) and Cout(co).**

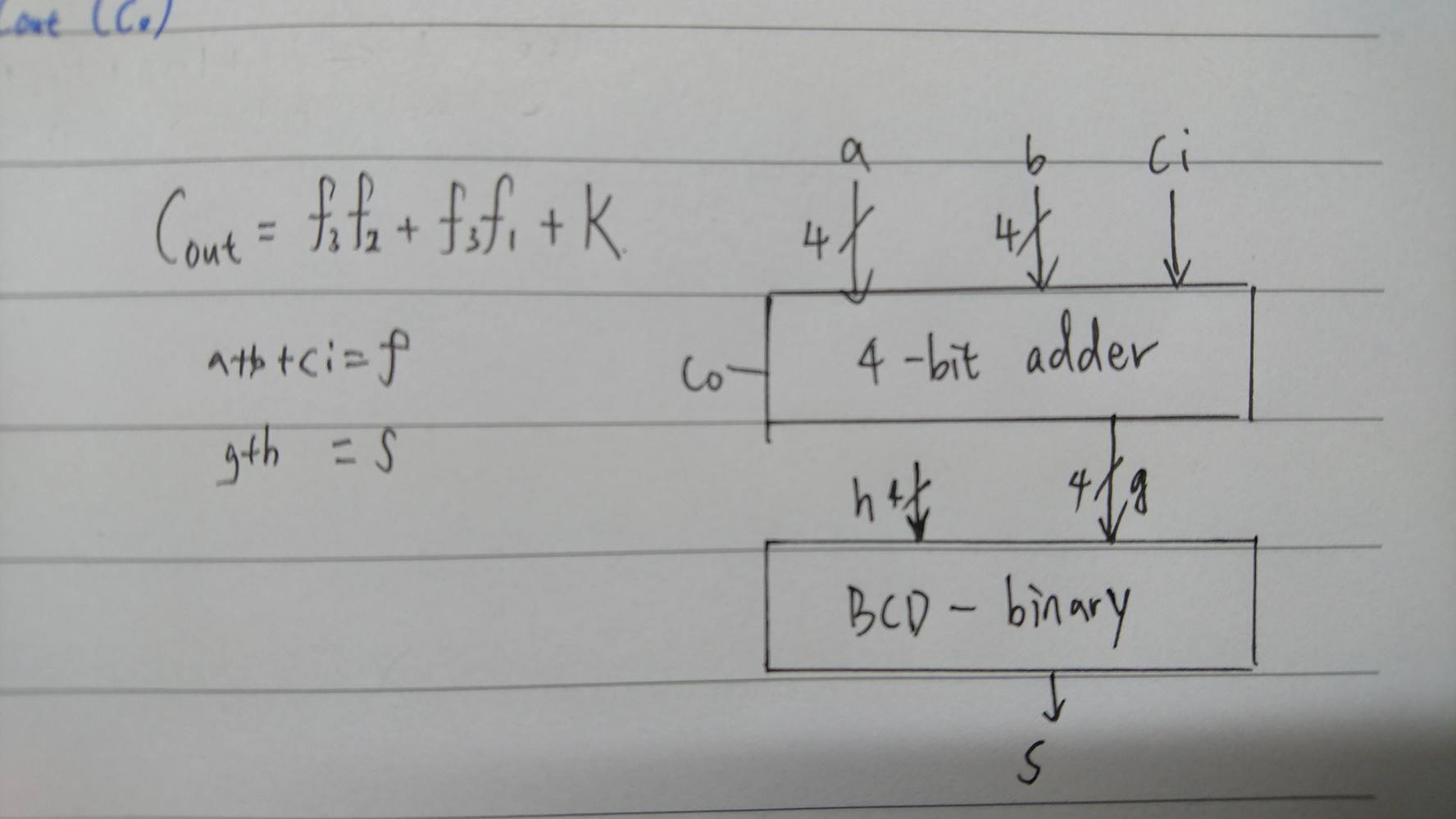
Design Specification

input : [3:0]a, [3:0]b,ci;

output : co, [3:0]s;

wire [4:0]f,[3:0]g,[3:0]h;

block diagram :



Design Implementation

Logic function :

f = a+b+ci;

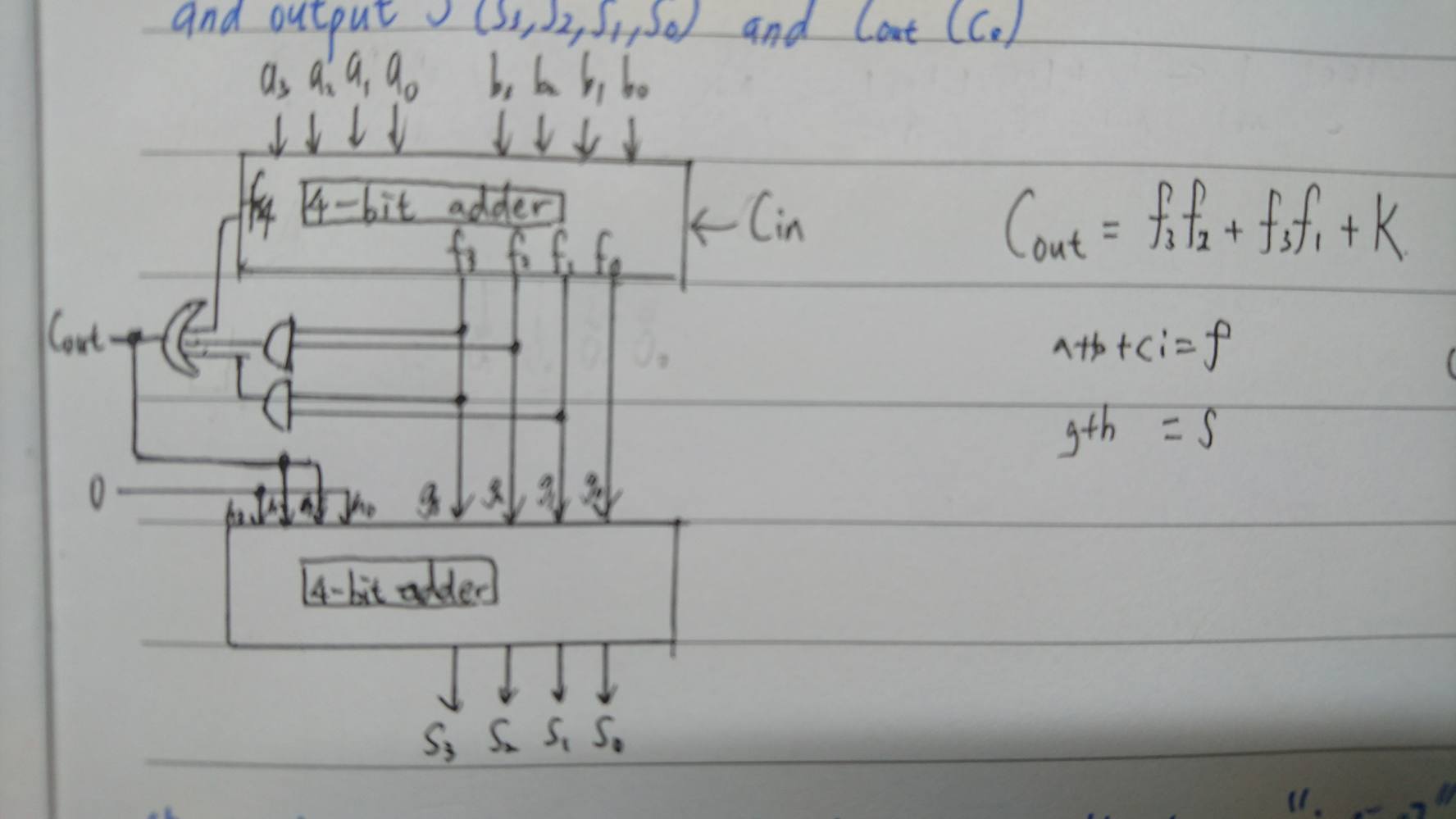
co = f[4]|(f[3]&f[2])|(f[3]&f[1]);

g[0] = f[0]; g[1] = f[1]; g[2] = f[2]; g[3] = f[3];

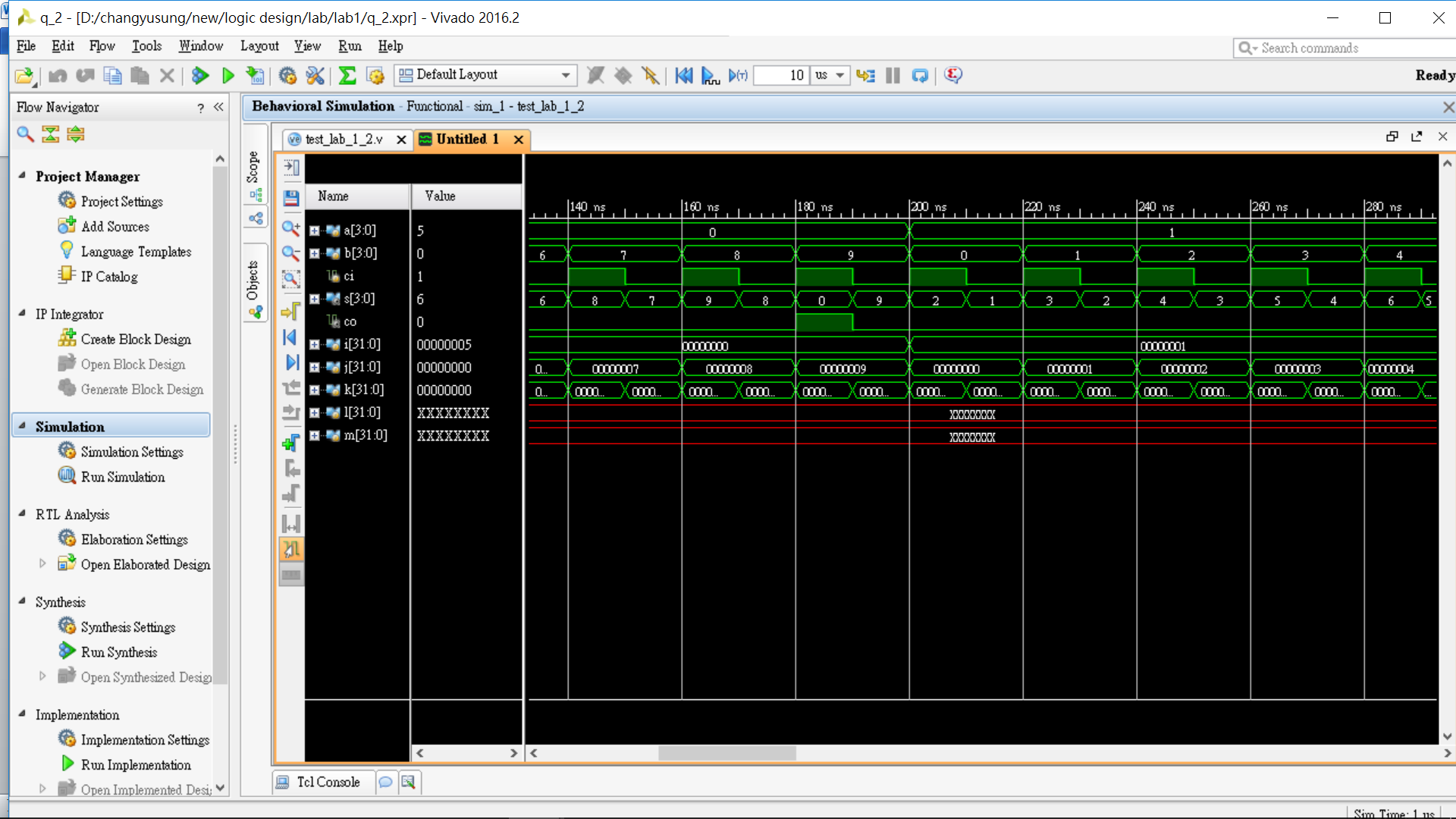
h[0] = 0; h[1] = co; h[2] = co; h[3] = 0;

s = g+h;

Logic diagram :



Result :



Discussion

1. 在打verilog時，a、b與f為多bits，”f = a+b+ci”這種形式是可以存在的，若有進位，程式軟體會自動幫助你進位，不用再詳細寫內部加法的過程，以此即可。
2. 當你覺得你的code沒有問題，但是模擬卻一直跑不太出來可能是你的修改次數過多，導致vivado讀不太到資料，因此只要重開一份project即可。

**3 (Bonus) Design a 3-to-8-line decoder with enable (input in[2:0], enable en and output d[7:0]).**

**3.1 Logic equation,**

**3.2 Logic schematic,**

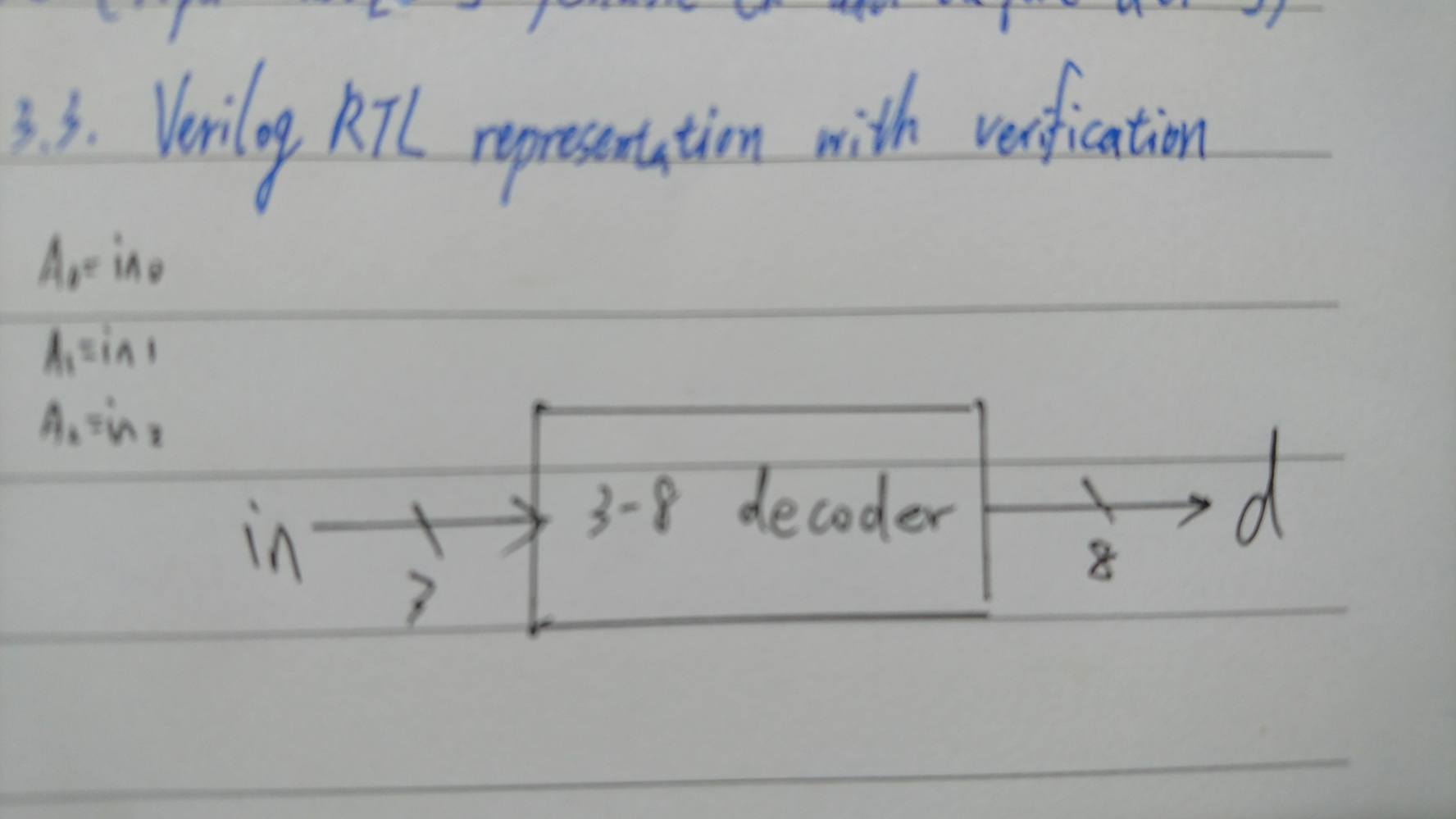
**3.3 Verilog RTL representation with verification.**

Design Specification

input : [2:0]in,en;

output : [7:0]d;

block diagram :



Design Implementation

Logic function :

d[0] = en&(~in[0])&(~in[1])&(~in[2]);

d[1] = en&(in[0])&(~in[1])&(~in[2]);

d[2] = en&(~in[0])&(in[1])&(~in[2]);

d[3] = en&(in[0])&(in[1])&(~in[2]);

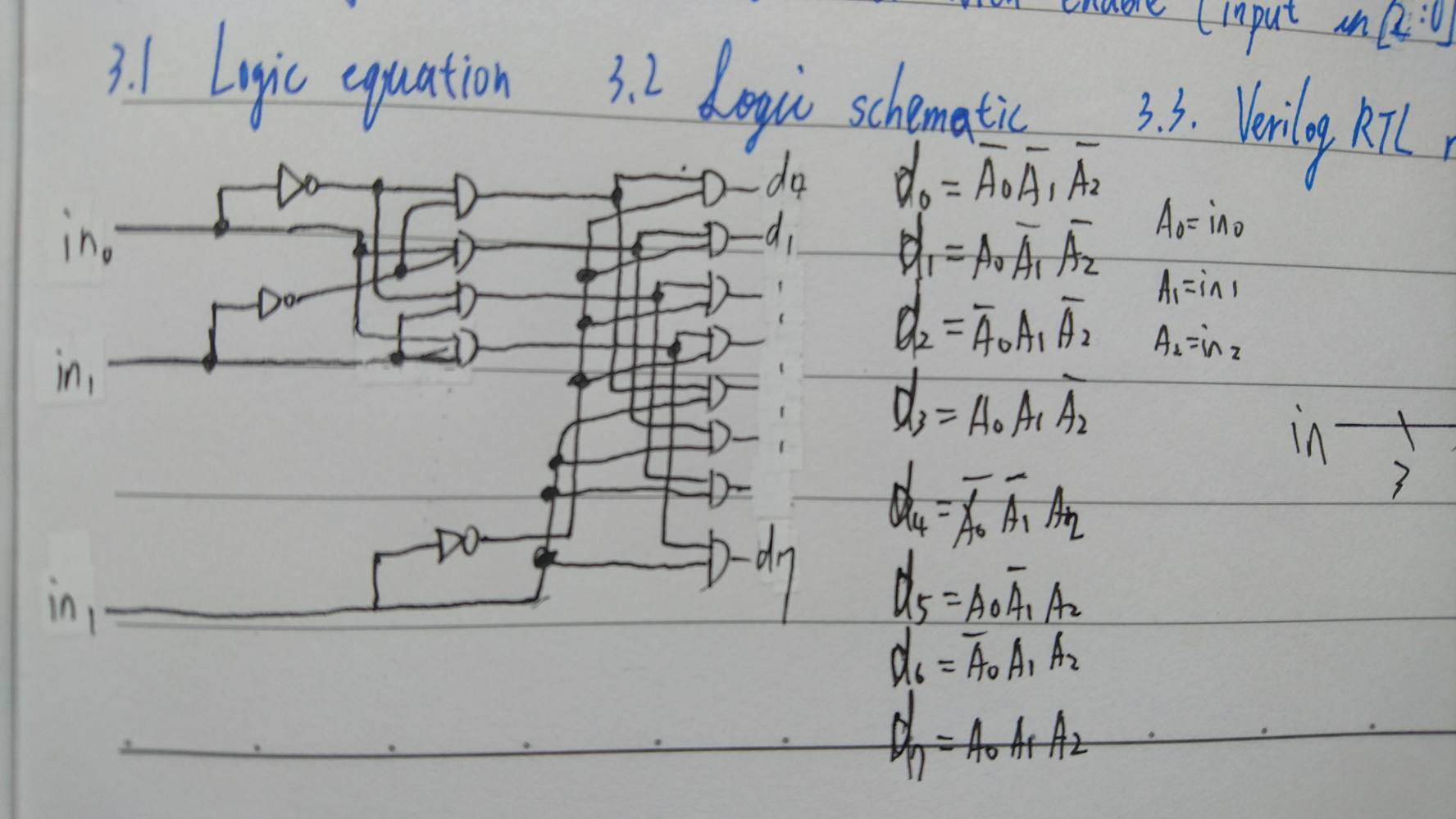
d[4] = en&(~in[0])&(~in[1])&(in[2]);

d[5] = en&(in[0])&(~in[1])&(in[2]);

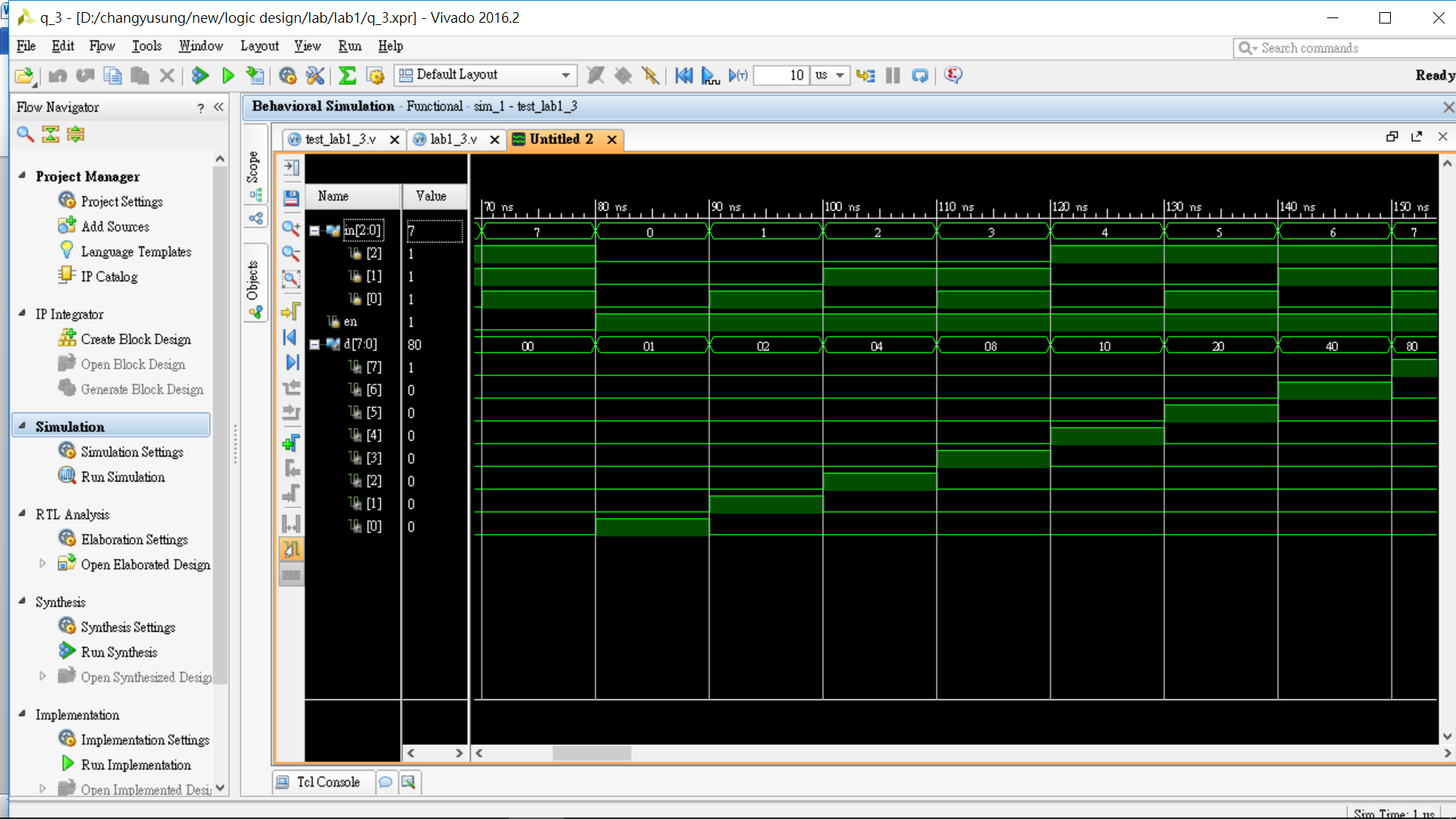
d[6] = en&(~in[0])&(in[1])&(in[2]);

d[7] = en&(in[0])&(in[1])&(in[2]);

Logic diagram :



Result :



Discussion

1. 當enable(en)=0時，output(d)不受input(in)影響；當en=1時，會把in進行解碼in=00🡪d=0001；in=01🡪d=0010；in=10🡪d=0100；in=11🡪d=1000

**Conclusion**：

這是繼上學期後再次打verilog，因為上學期我覺得我沒有學得很好，因此這次我學得更加的認真，而這次打verilog也讓我收穫很多，再次習得如何打verilog，也很開心，能夠把自己做的logic diagram打成verilog，真的是挺開心的。