Lab 6: Simple Calculator

Objective

- ✓ Review arithmetic functions.
- ✓ Learn simple calculator.

Prerequisite

- ✓ Fundamentals of logic design.
- ✓ Logic modeling in Verilog HDL.

Pre-labs

1 Implement a scan function to catch the keypad press.
   1.1 Write the spec (inputs, outputs, and function table, state diagram) of the design.
   1.2 Draw the related block/logic diagram.
   1.3 Use Verilog to implement 1.2 and verify the design with simulation results.

Experiments

1 Implement the keypad press catch function with the FPGA demo board.

2 Implement a single digit decimal adder using the keypad as the input, push button as the plus function, and display the results on the 14-segment display (The first two digit are the addend/augend, and the last two digits are the sum).

3 Implement a two-digit decimal adder/subtractor.

4 (Bonus) Implement a simple calculator for 1-digit calculation of addition, subtraction, and multiplication using the keypad as the input. When calculation, press 'A' for addition, 'D' for subtraction, and 'B' for multiplication.
   4.1 Use the binary addition/multiplication as the computing core.
   4.2 Include a binary-to-decimal converter as the display conversion.

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