Lab 11: LCD Display (1)

Objective

- ✓ Implement the timer and stopwatch functions of the electronic clock.

Prerequisite

- ✓ Fundamentals of logic gates.
- ✓ Logic modeling in Verilog HDL.
- ✓ Simple logic development and FSM control

Experiments

1 LCD display example.
  - 1.1 Follow the lecture. Create the ROM block to store the graphs given in the example file "picture.coe". There are 16 64x64 pictures but the last 7 are empty. Study the file.
  - 1.2 Integrate the given example files "ct_clkdivider.v", "rom_ctrl.v", "lcd_ctrl.v", "lcd_display.v", and use the given pin assignment file "lcd_display.ucf" to build the whole LCD display example.
  - 1.3 The animation displays 10 pictures repeatedly. Among them, the 10th picture is an empty one. Fix the design to show 9 pictures repeatedly and ignore the 10th picture. Therefore, the result animation will be smoother.
  - 1.4 Modify the design by inserting an additional 2-second delay after showing the last (9th) picture. You should do that by adding one extra state with a pause counter.

2 (Bonus) Modify the pictures and put your signature on top of the given animation. You can use the space around. You name can be either English or Chinese.

TA: _____

