邏輯設計實驗 Lab12 結報

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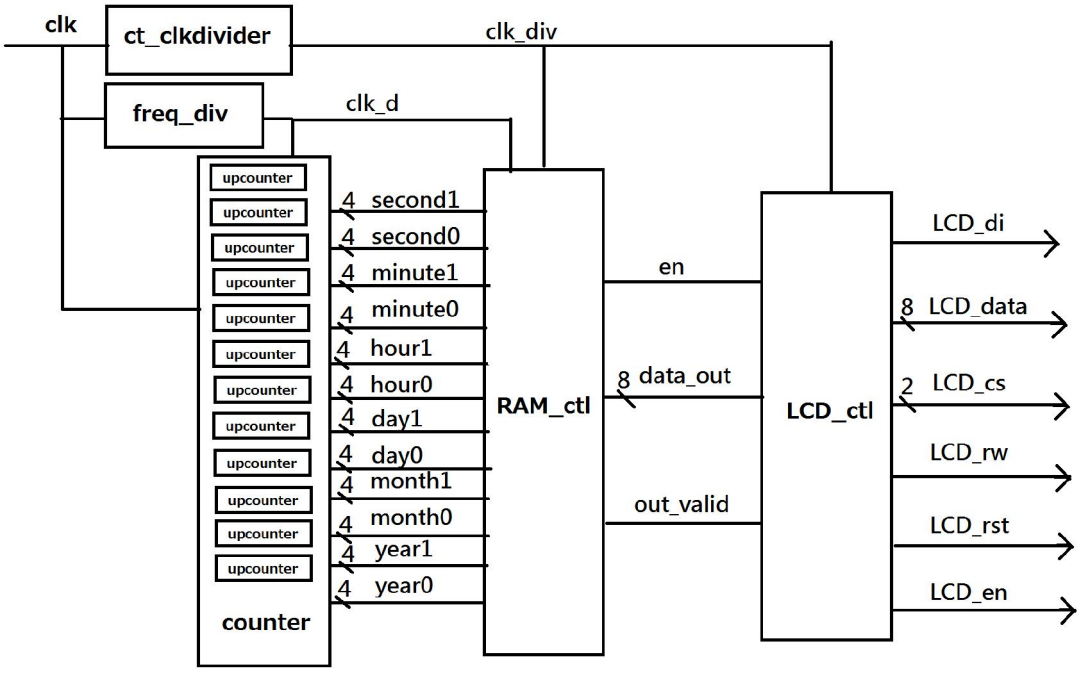
1 For the time delay of electronic clock in lab7. Instead using 14-segment displays to show the time, use LCD to present all the functions in lab7.

Design Specification

```
input    clk,
input    rst_n,

output   LCD_rst,
output wire   [1:0] LCD_cs,
output   LCD_rw,
output   LCD_di,
output wire   [7:0] LCD_data,
output   LCD_en
wire     [3:0]second1,second0,minute1,minute0,hour1,hour0,day1,day0,month1,
         month0,year1,year0;
wire en,out_valid;
wire     [7:0] data_out;
wire     clk_div;
wire     clk_d;
```

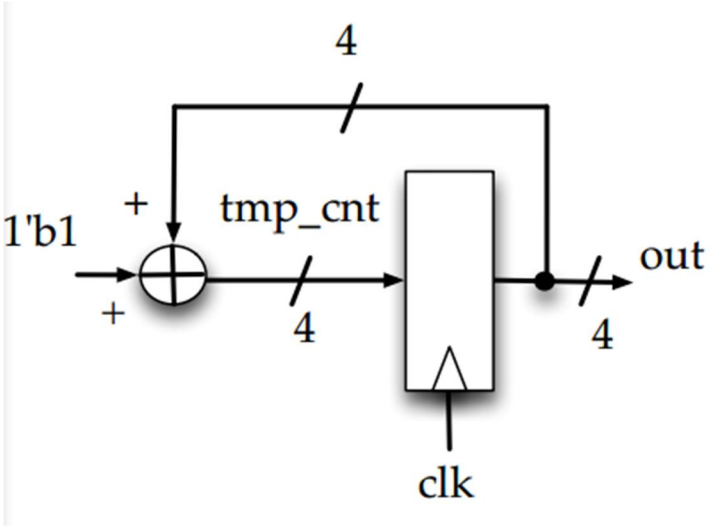
block diagram:



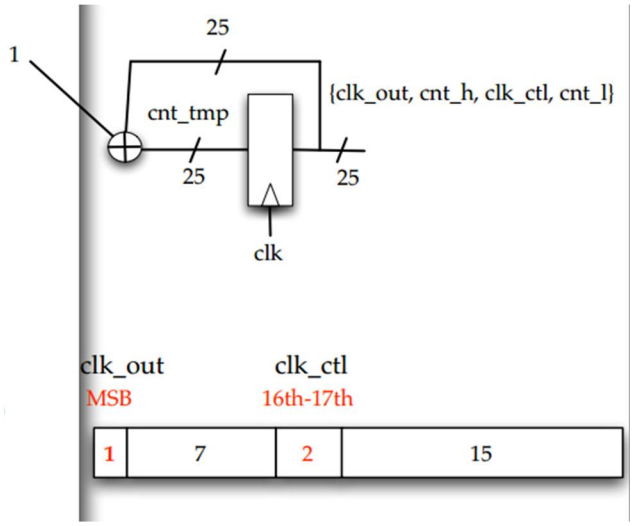
Design Implementation

logic function / logic diagram:

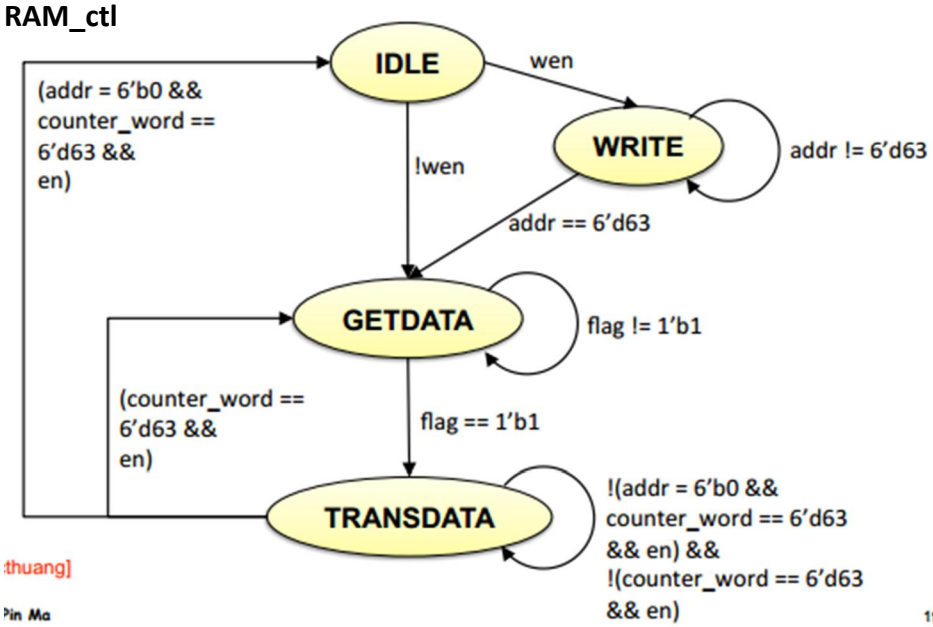
upcounter

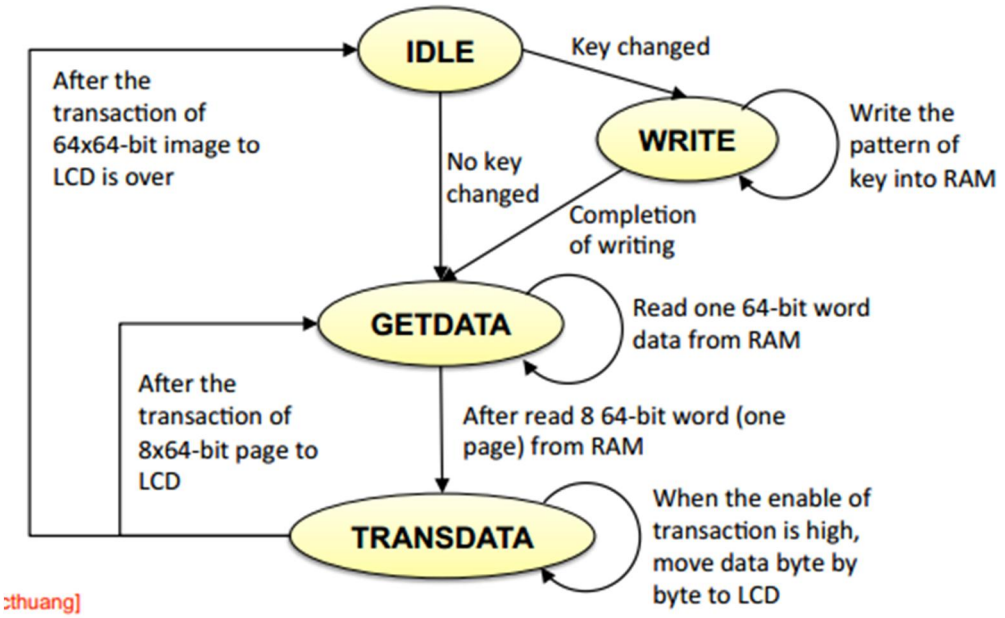


freq_div:

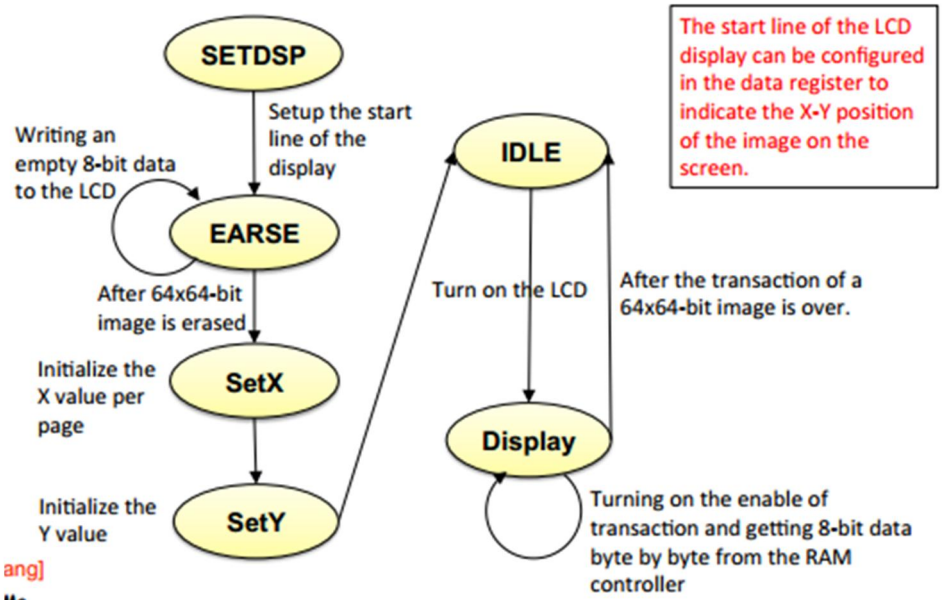


RAM_ctl





LCD_ctl



counter

連接 second, minute, hour, day, month, year 的 counter, 設定 second 從 0 數到 59 進位至 minute，minute 從 0 數到 59 進位至 hour，hour 從 day0 數到 23 進位至 day，day 從 1 數到 monthday(28or30or31)進位至 month，month 從 1 數到 12 進位至 year，year 從 0 數到 99。

I/O pin assignment:

```
## pin mapping
NET "clk"                LOC = "R10";
NET "rst_n"              LOC = "N3";

## LCD control signals
NET "LCD_rst"            LOC = "E3";
NET "LCD_cs[1]"          LOC = "E1";
NET "LCD_cs[0]"          LOC = "F4";
NET "LCD_data[7]"        LOC = "F3";
NET "LCD_data[6]"        LOC = "D2";
NET "LCD_data[5]"        LOC = "D1";
NET "LCD_data[4]"        LOC = "H7";
NET "LCD_data[3]"        LOC = "G6";
NET "LCD_data[2]"        LOC = "E4";
NET "LCD_data[1]"        LOC = "D3";
NET "LCD_data[0]"        LOC = "F6";
NET "LCD_en"              LOC = "F5";
NET "LCD_rw"              LOC = "C2";
NET "LCD_di"             LOC = "C1";
```

Discussion:

利用 RAM 自 counter 讀取資料並輸出在 LCD 上。

Conclusion:

只要結合 lab07 的 counter 與 RAM 便可製作簡易的電子鐘。