

# 邏輯設計實驗 Lab11 結報

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## 1 LCD display example.

**1.1** Follow the lecture. Create the ROM block to given in the example file “picture.coe”. There are the last 7 are empty. Study the file.

**1.2** Integrate the given example files “ct\_clkdivi “lcd\_ctrl.v”, lcd\_display.v”, and use the given pin assignment the “lcd\_display.ucf” to build the whole LCD display example.

**1.3** The animation displays 10 pictures repeatedly. Among them, the 10<sup>th</sup> picture is an empty one. Fix the design to show 9 pictures repeatedly and ignore the 10<sup>th</sup> picture. Therefore, the result animation will be smoother.

**1.4** Modify the design by inserting an additional 2-second delay after showing the last (9<sup>th</sup>) picture. You should do that by adding one extra state with a pause counter.

Design Specification:(2/2)  
block diagram of the design or Logic Diagram:(8/8)  
I/O pin assignment :(2/2)  
Discussion +Conclusion:(3/3)  
Function explanation:(6/10)

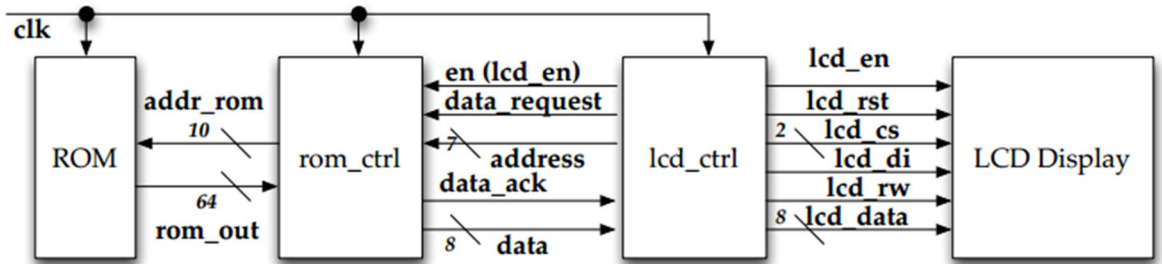
## Design Specification

**output :** lcd\_rst; // LCD reset  
[1:0] lcd\_cs; // LCD frame selection  
lcd\_rw; // LCD read/write control  
lcd\_di; // LCD data/instruction  
[7:0] lcd\_d; // LCD data  
lcd\_e; // LCD enable  
data\_ack; //data re-arrangement buffer ready indicator  
data\_request; // request for the memory data

**input :** clk, // clock from crystal  
rst\_n, // active low reset

**wire :** clk\_50k; // Divided 50k clock  
clk\_d;  
[7:0] data; // byte data transfer from buffer  
[6:0] addr; // Address for each picture

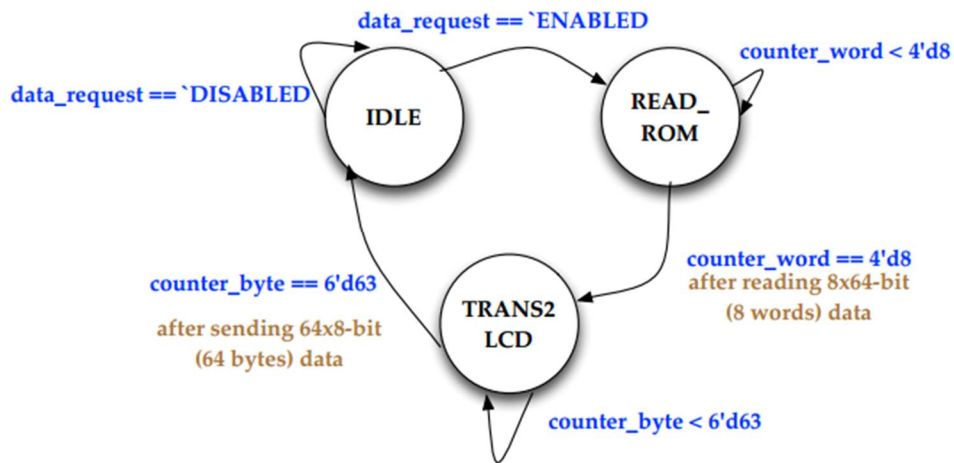
block diagram:



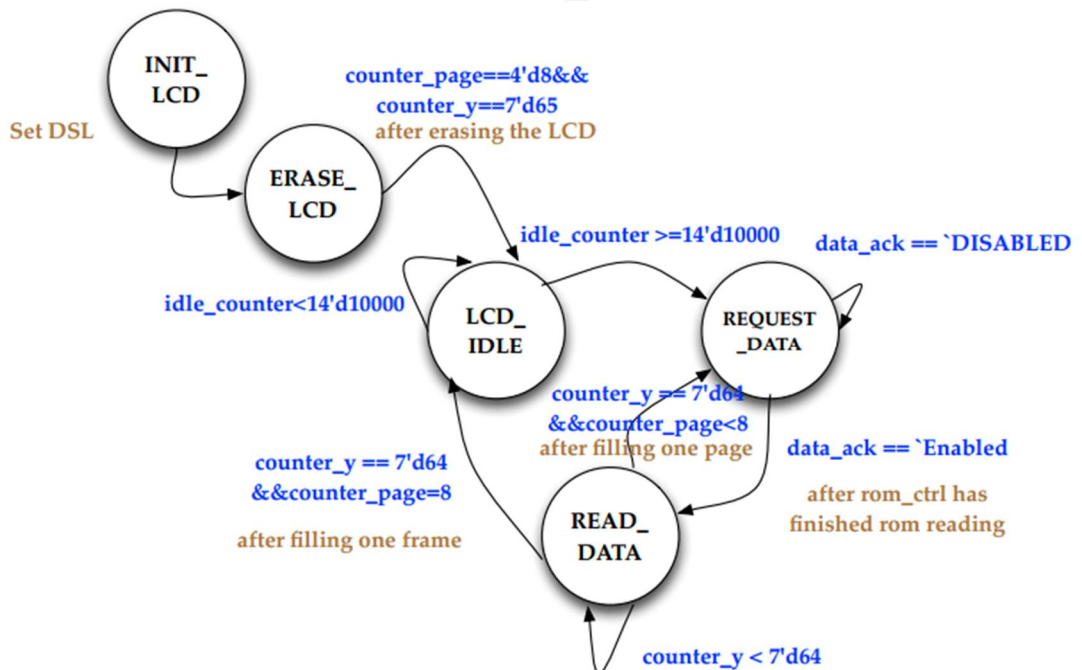
## Design Implementation

logic function / logic diagram:

*rom\_ctl:*



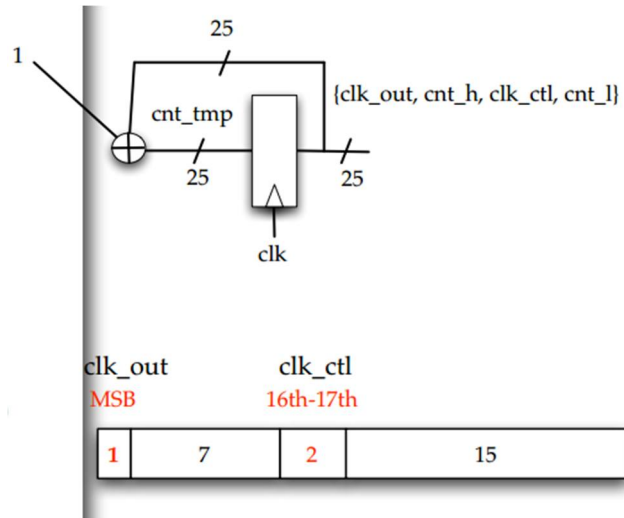
*lcd\_ctl:*



**clock\_divider:**

將 40MHz 的 clk divide 成 50kHz

**freq\_div:**



用 1Hz 控制 lcd\_ctl 中 LCD\_PAUSE state 的 cnt，使當 LCD 顯示第 8 張圖時，停留兩秒後再返回第一張。

**I/O pin assignment:**

## pin mapping

```
NET "clk" LOC = "R10";  
NET "rst_n" LOC = "N3";
```

## LCD control signals

```
NET "LCD_RST" LOC = "E3";  
NET "LCD_CS[1]" LOC = "E1";  
NET "LCD_CS[0]" LOC = "F4";  
NET "LCD_D[7]" LOC = "F3";  
NET "LCD_D[6]" LOC = "D2";  
NET "LCD_D[5]" LOC = "D1";  
NET "LCD_D[4]" LOC = "H7";  
NET "LCD_D[3]" LOC = "G6";  
NET "LCD_D[2]" LOC = "E4";  
NET "LCD_D[1]" LOC = "D3";  
NET "LCD_D[0]" LOC = "F6";  
NET "LCD_E" LOC = "F5";  
NET "LCD_RW" LOC = "C2";  
NET "LCD_DI" LOC = "C1";
```

NET "data\_request" LOC = "H5";

NET "data\_ack" LOC = "H6";

### Discussion:

設置一 counter 使其自動改變音高並結合 speaker\_ctl 和 buzzer\_ctl 產生一段旋律。

bonus:2

**2 (Bonus) Modify the pictures and put your signature on top of the given animation. You can use the space around. You name can be either English or Chinese.**

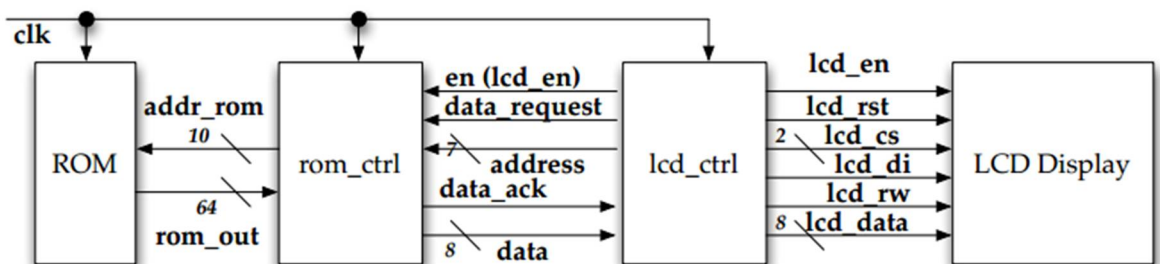
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lcd\_e; // LCD enable  
data\_ack; //data re-arrangement buffer ready indicator  
data\_request; // request for the memory data

**input :** clk, // clock from crystal  
rst\_n, // active low reset

**wire :** clk\_50k; // Divided 50k clock  
clk\_d;  
[7:0] data; // byte data transfer from buffer  
[6:0] addr; // Address for each picture

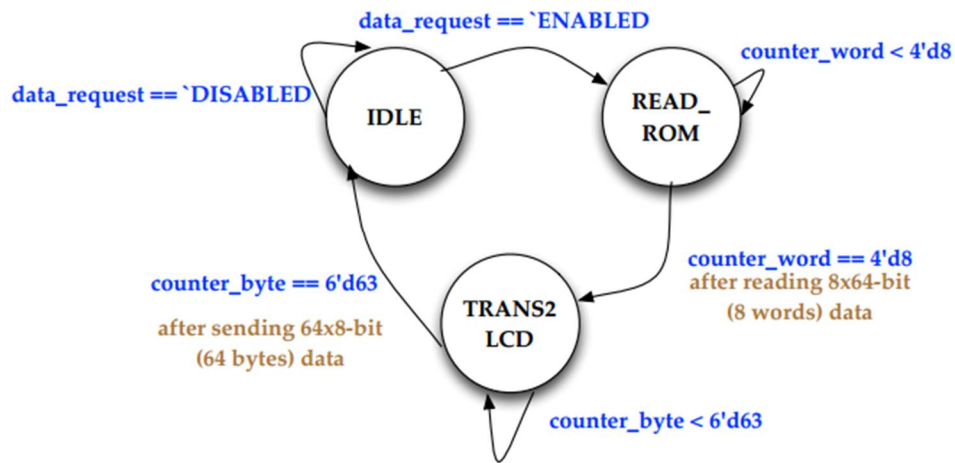
block diagram:



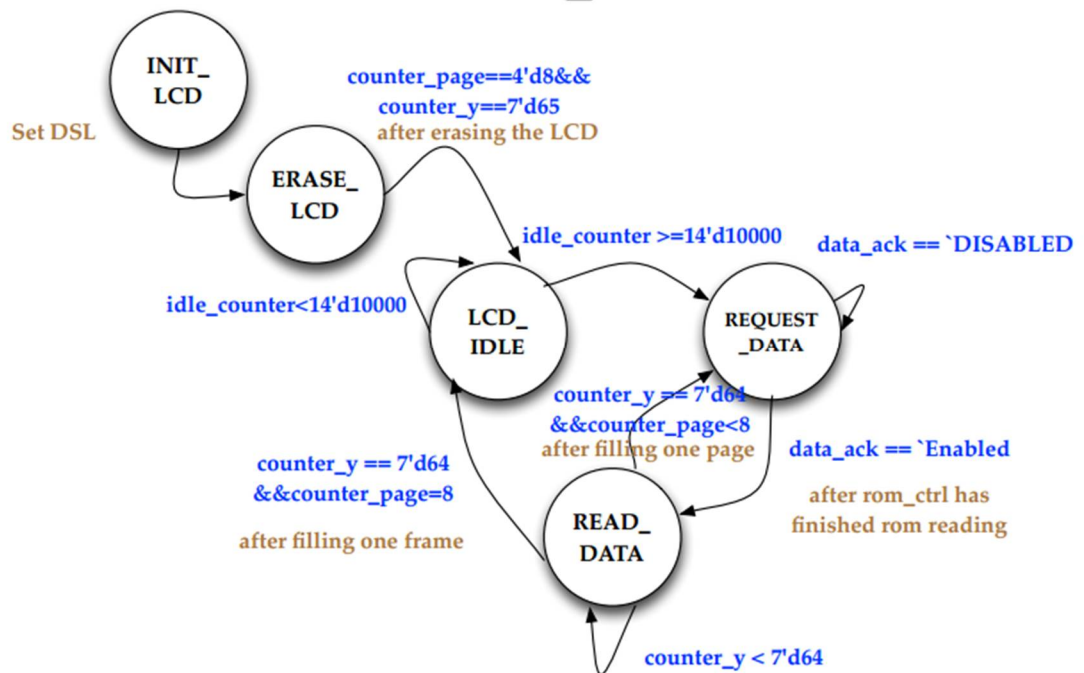
## Design Implementation

logic function / logic diagram:

*rom\_ctl:*

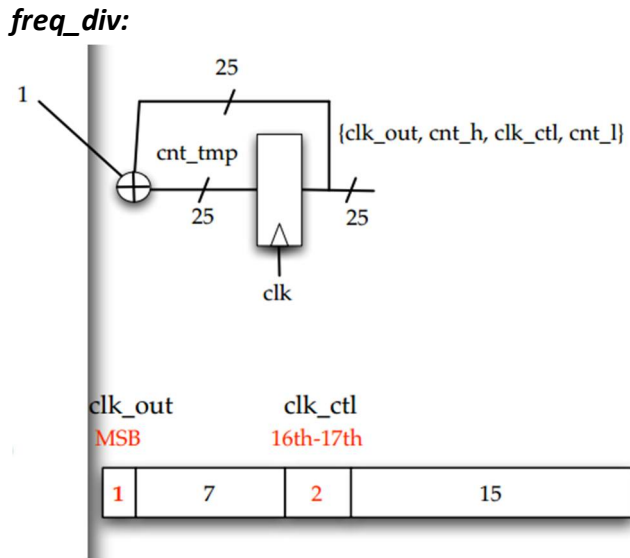


*lcd\_ctl:*



*clock\_divider:*

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NET "LCD\_D[6]" LOC = "D2";

NET "LCD\_D[5]" LOC = "D1";

NET "LCD\_D[4]" LOC = "H7";

NET "LCD\_D[3]" LOC = "G6";

NET "LCD\_D[2]" LOC = "E4";

NET "LCD\_D[1]" LOC = "D3";

NET "LCD\_D[0]" LOC = "F6";

NET "LCD\_E" LOC = "F5";

NET "LCD\_RW" LOC = "C2";

NET "LCD\_DI" LOC = "C1";

NET "data\_request" LOC = "H5";

NET "data\_ack" LOC = "H6";

**Discussion:**

同 lab11\_1，利用 notepad 更改 coe 檔的圖。

**Conclusion:**

利用 ROM 去讀取圖片以顯示在 LCD 上。