

邏輯設計實驗 Lab07 結報

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1 Finish the time display function supporting 24-hour (00-23).

1.1 Support two modes: AM/PM and 24-hour.

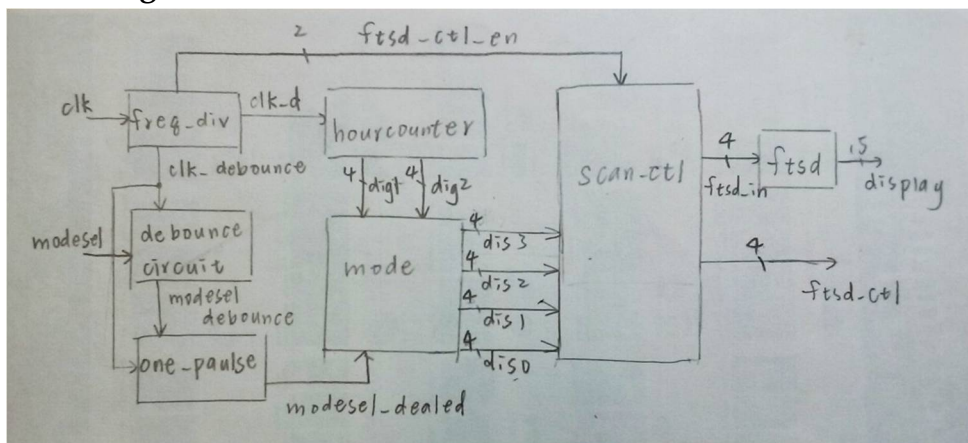
Design Specification

output : [3:0] ftsd_ctl, [14:0] display

input : clk, modesel, rst_n

wire : modesel_debounce, modesel_dealed, clk_d, [1:0]ftsd_ctl_en, [3:0]digit0, [3:0]digit1, count_enable, [3:0]ftsd_in, [3:0] dis0, [3:0]dis1, [3:0]dis2, [3:0]dis3, clk_debounce

block diagram:



Design Implementation

logic function / logic diagram:

upcounter

7-1

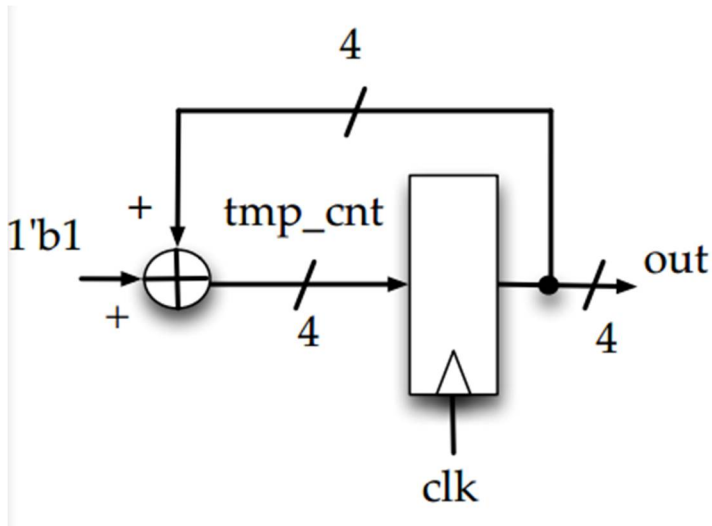
Design specification(2/2)

Block diagram or logic diagram of the design(4/4)

I/O pin assignment(1/1)

Discussion+conclusion(3/3)

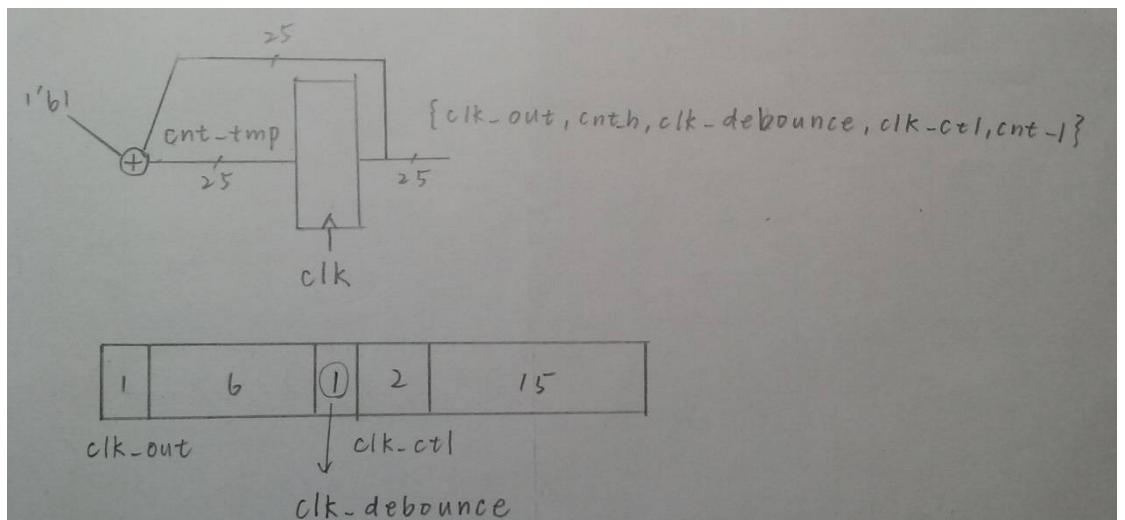
Function explanation(5/5)



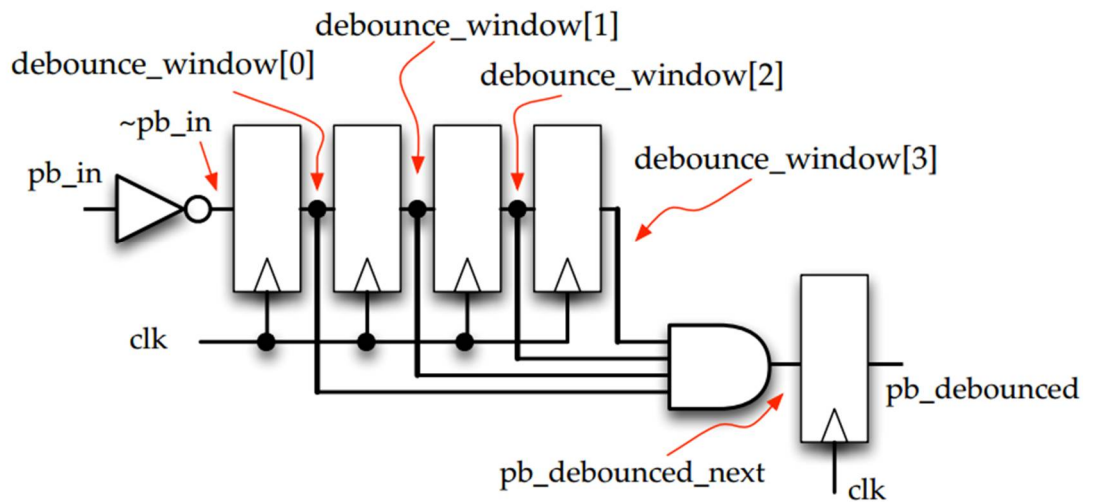
hourcounter

結合兩個 upcounter，從 00 數到 23

freq_div:

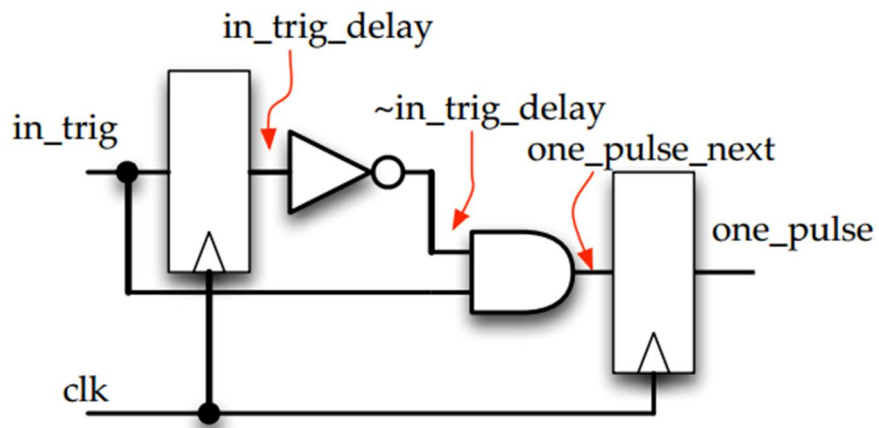


debounce_circuit



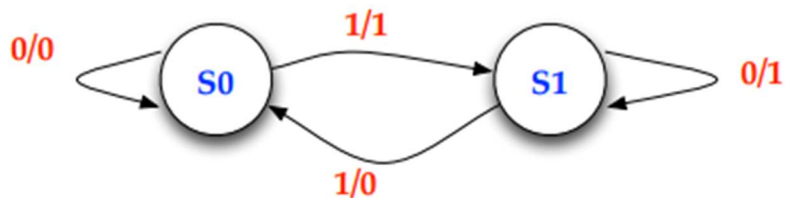
When all 4 bits of the registers are high the output of the debounce circuit changes to high

one_pulse



When one presses the push button for a short moment, the time that the switch is closed (ms range) is usually much longer than one clock period (μ s or ns range). The one-pulse circuit generates only a one-clockperiod-long pulse every time the push button is hit, independent of the time one keeps the button pressed

fsm



scan_ctl

if ftsd_ctl_en=00
->控制第一個 14 段顯示器
if ftsd_ctl_en=01

->控制第二個 14 段顯示器

if ftsd_ctl_en=10

->控制第三個 14 段顯示器

if ftsd_ctl_en=11

->控制第四個 14 段顯示器

mode

```
當 bcd=4'd0: display = 15'b0000_0011_1111_111; //0
當 bcd=4'd1: display = 15'b1111_1111_1011_011; //1
當 bcd=4'd2: display = 15'b0010_0100_1111_111; //2
當 bcd=4'd3: display = 15'b0000_1100_1111_111; //3
當 bcd=4'd4: display = 15'b1001_1000_1111_111; //4
當 bcd=4'd5: display = 15'b0100_1000_1111_111; //5
當 bcd=4'd6: display = 15'b0100_0000_1111_111; //6
當 bcd=4'd7: display = 15'b0001_1111_1111_111; //7
當 bcd=4'd8: display = 15'b0000_0000_1111_111; //8
當 bcd=4'd9: display = 15'b0000_1000_1111_111; //9
default: display = 15'b1111_1111_1111_111; //DEF
```

I/O pin assignment:

```
NET "clk" LOC = R10;
NET "rst_n" LOC = T2;
NET "modesel" LOC = N3;
NET "ftsd_ctl[0]" LOC = V8;
NET "ftsd_ctl[1]" LOC = U8;
NET "ftsd_ctl[2]" LOC = V6;
NET "ftsd_ctl[3]" LOC = T6;
NET "display[0]" LOC = U5;
NET "display[1]" LOC = T7;
NET "display[2]" LOC = R7;
NET "display[3]" LOC = V7;
NET "display[4]" LOC = V4;
NET "display[5]" LOC = T4;
NET "display[6]" LOC = T3;
NET "display[7]" LOC = R5;
NET "display[8]" LOC = N5;
NET "display[9]" LOC = R3;
NET "display[10]" LOC = U7;
```

NET "display[11]" LOC = T5;
 NET "display[12]" LOC = V5;
 NET "display[13]" LOC = N4;
 NET "display[14]" LOC = P6;

7-2
 Design specification(3/3)
 Block diagram or logic diagram of the design(5/5)
 I/O pin assignment(2/2)
 Discussion+conclusion(5/5)
 Function explanation(5/5)

Discussion:

設置一個 fsm 去切換 ampm 制或 24 小時制，須注意的為凌晨 12 點是 am，中午 12 點為 pm，所以 ampm 皆從 12 開始回歸到 1 再繼續數到 11。

2 For the date functions in clock (no leap year), we have the following functions:

- o Day (Jan/March/May/July/Aug/Oct/Dec: 1-31, Feb: 28, Apr/June/Sept/Nov: 30),
- o Month (1-12),
- o Year (00-99).

Implement the following functions:

2.1 Month-Day function display in the 4 14-segment displays.

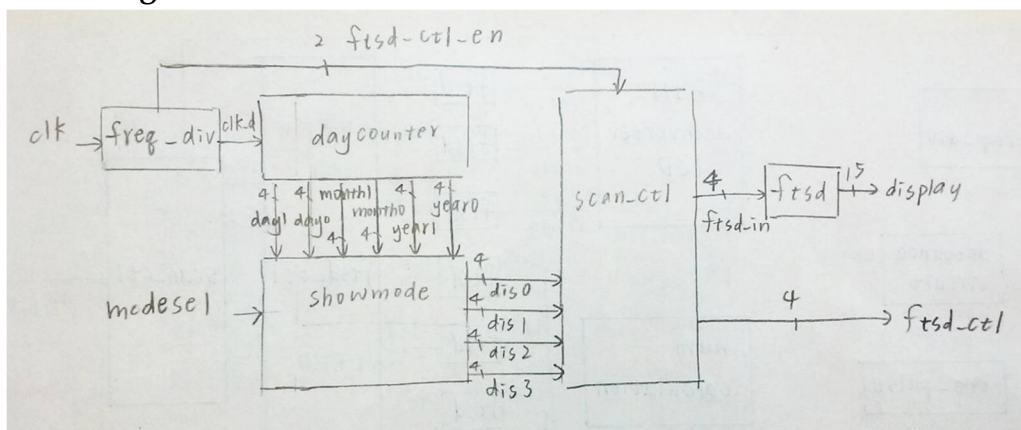
2.2 Combine the Year and 1.1 to finish a Year-Month-Day timer, and use one DIP switch to select the display of Year (2 14SD) or Month-Day (4 14SD).

output : [3:0] ftsd_ctl, [14:0] display

input : clk, modesel, rst_n

wire : clk_d, [1:0]ftsd_ctl_en, [3:0] day0, [3:0] day1, [3:0] month0, [3:0] month1, [3:0] year0, [3:0] year1, count_enable, [3:0]ftsd_in, [3:0] dis0, [3:0]dis1, [3:0]dis2, [3:0]dis3

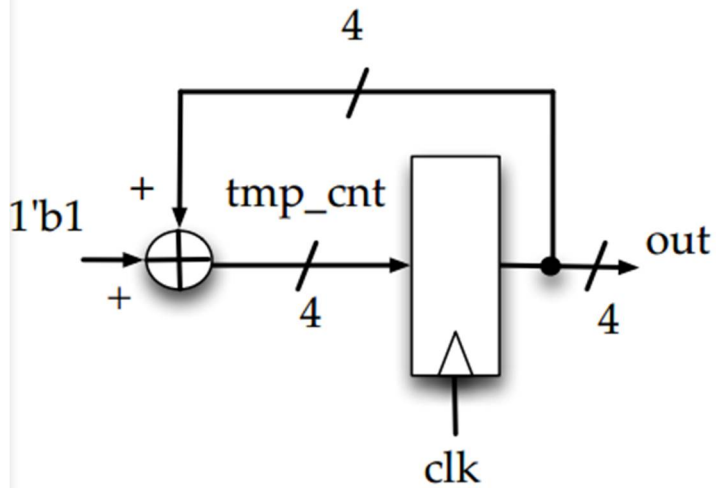
block diagram:



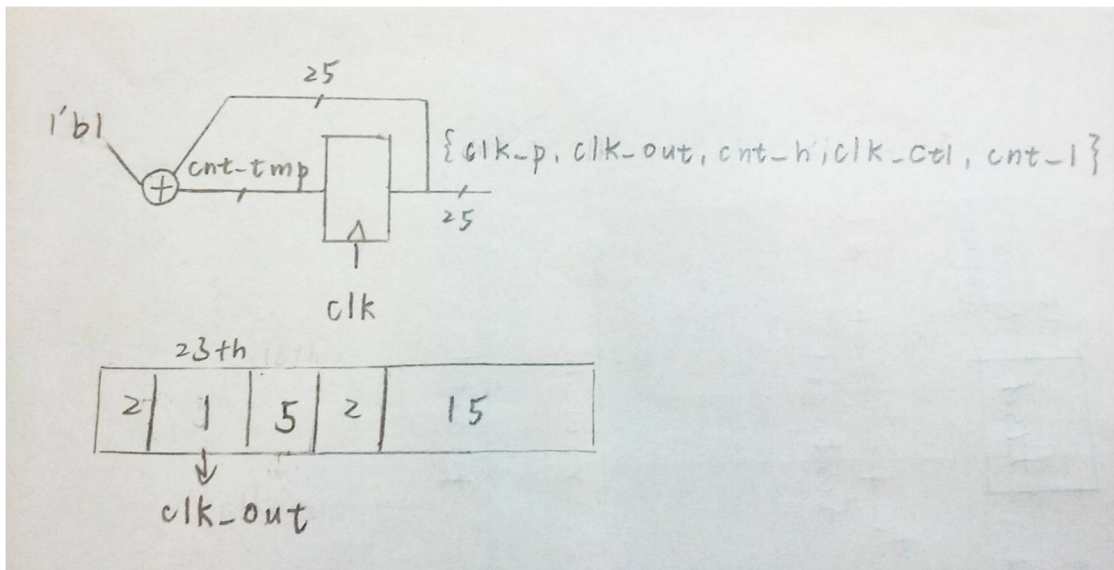
Design Implementation

logic function / logic diagram:

upcounter



freq_div:



scan_ctl

if ftsd_ctl_en=00

->控制第一個 14 段顯示器

if ftsd_ctl_en=01

->控制第二個 14 段顯示器

if ftsd_ctl_en=10

->控制第三個 14 段顯示器

if ftsd_ctl_en=11

->控制第四個 14 段顯示器

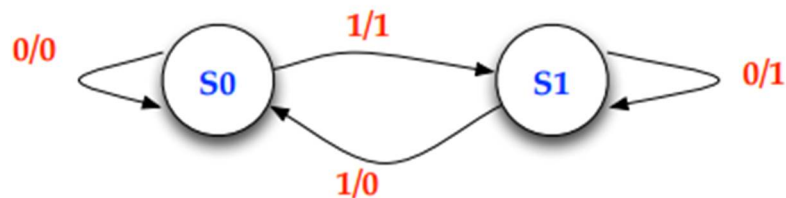
ftsd

```
當 bcd=4'd0: display = 15'b0000_0011_1111_111; //0  
當 bcd=4'd1: display = 15'b1111_1111_1011_011; //1  
當 bcd=4'd2: display = 15'b0010_0100_1111_111; //2  
當 bcd=4'd3: display = 15'b0000_1100_1111_111; //3  
當 bcd=4'd4: display = 15'b1001_1000_1111_111; //4  
當 bcd=4'd5: display = 15'b0100_1000_1111_111; //5  
當 bcd=4'd6: display = 15'b0100_0000_1111_111; //6  
當 bcd=4'd7: display = 15'b0001_1111_1111_111; //7  
當 bcd=4'd8: display = 15'b0000_0000_1111_111; //8  
當 bcd=4'd9: display = 15'b0000_1000_1111_111; //9  
default: display = 15'b1111_1111_1111_111; //DEF
```

daycounter

每個月會有不同的日期，利用 `load_def_day` 決定是否增加一個月，`load_def_month` 決定是否增加一年。

showmode



I/O pin assignment:

```
NET "clk" LOC = R10;  
NET "rst_n" LOC = T2;  
NET "modesel" LOC = T1;  
NET "ftsd_ctl[0]" LOC = V8;  
NET "ftsd_ctl[1]" LOC = U8;  
NET "ftsd_ctl[2]" LOC = V6;  
NET "ftsd_ctl[3]" LOC = T6;
```

```
NET "display[0]" LOC = U5;  
NET "display[1]" LOC = T7;  
NET "display[2]" LOC = R7;  
NET "display[3]" LOC = V7;  
NET "display[4]" LOC = V4;  
NET "display[5]" LOC = T4;  
NET "display[6]" LOC = T3;  
NET "display[7]" LOC = R5;  
NET "display[8]" LOC = N5;  
NET "display[9]" LOC = R3;  
NET "display[10]" LOC = U7;  
NET "display[11]" LOC = T5;  
NET "display[12]" LOC = V5;  
NET "display[13]" LOC = N4;  
NET "display[14]" LOC = P6;
```

Discussion:

為了方便觀察，將速度調快約 4 倍。

Conclusion:

lab07 相較於前面的實驗較簡單，只是不斷運用 upcounter 的概念，只要注意一些基本時間運算的規則即可。