邏輯設計實驗 Lab06 預報

104060012 邱怡庭

1 Implement a scan function to catch the keypad press.

1.1 Write the spec (inputs, outputs, and function table, state diagram) of the design.

input clk; // scan clock

input rst_n; // active low reset

input [3:0] col_n; // pressed_detected col_numn index

output [3:0] row_n; // scanned row_n index

output [3:0] key; // returned pressed_detected key

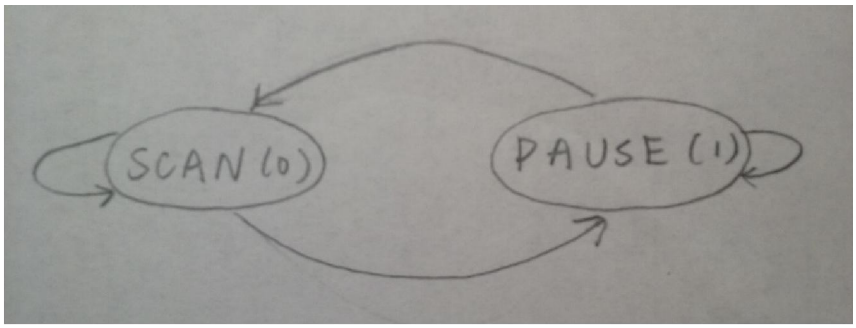
output pressed; // whether key_detected pressed_detected (1) or not (0)

output [3:0]key_detected; //for check

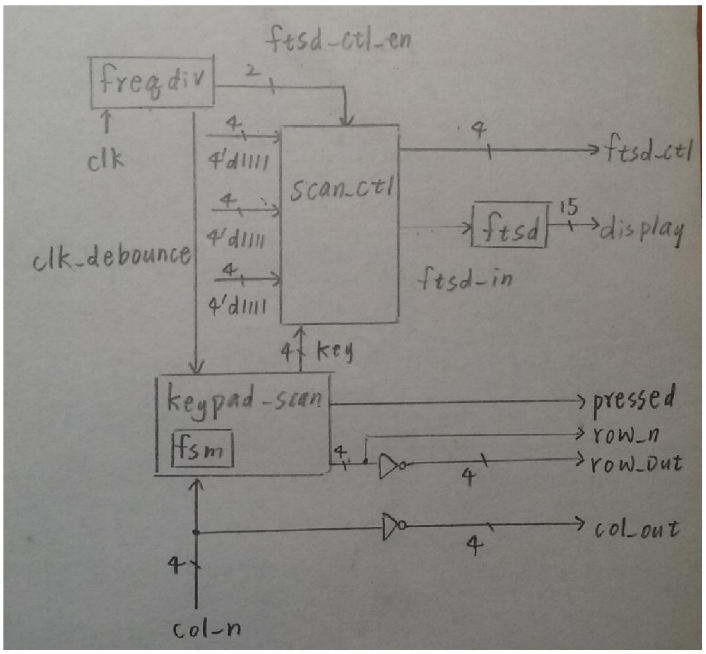
function table

Row	Column	Key
0111	0111	F
0111	1011	E
0111	1101	D
0111	1110	C
1011	0111	B
1011	1011	3
1011	1101	6
1011	1110	9
1101	0111	A
1101	1011	2
1101	1101	5
1101	1110	8
1110	0111	0
1110	1011	1
1110	1101	4
1110	1110	7

state diagram



1.2 Draw the related block/logic diagram.



1.3 Use Verilog to implement 1.2 and verify the design with simulation