pre lab(10)
Draw the logic diagram (5/5)
Construct Verilog RTL representation for the logics with verification (5/5)

邏輯設計實驗 Lab02 預報

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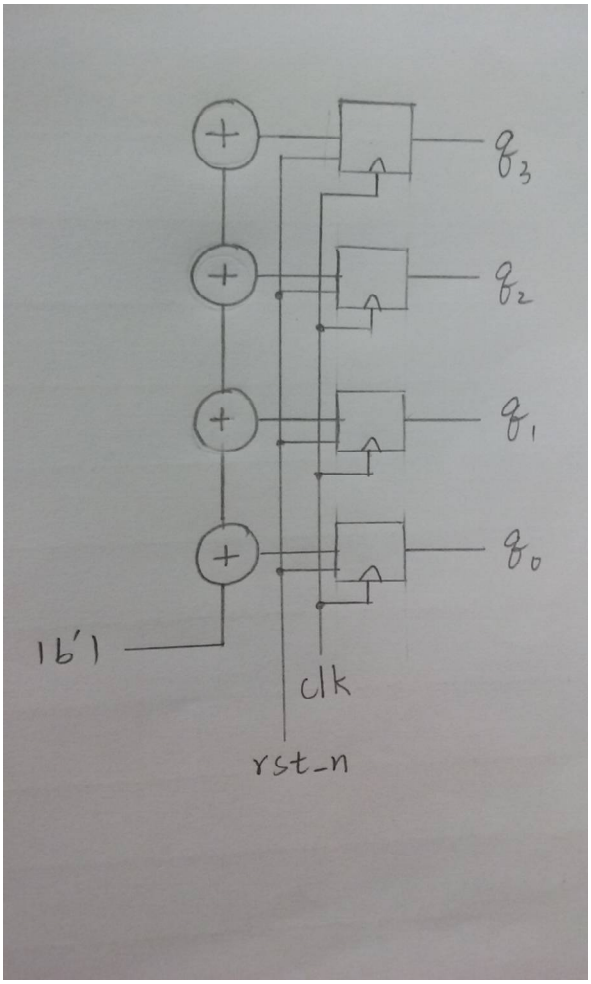
1 Consider a 4-bit synchronous binary up counter.

1.1 Draw the logic diagram



1.2 Construct Verilog RTL representation for the logics with verification.

The Final Result: