邏輯設計實驗 Lab01 結報

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34+10=44

1 Design and implement a full adder. (s+cout=x+y+cin)

1.1 Write the logic equation.
1.2 Draw the related logic diagram.
1.3 Verilog RTL representation with verification.

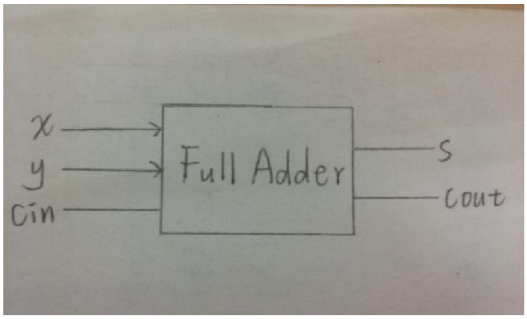
Design Specification

2/2

Input:x,y,cin

Output:s,cout

block diagram:



Design Implementation

logic function:

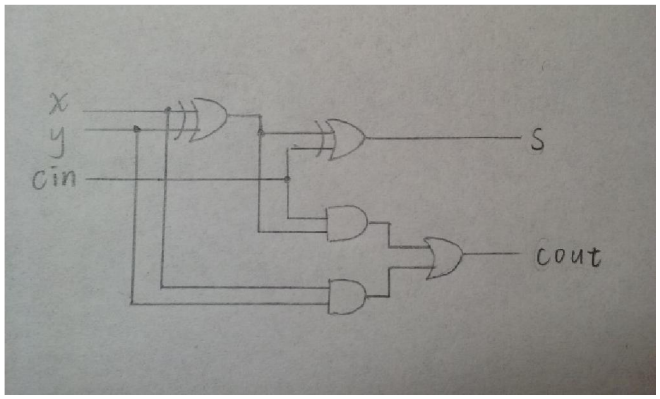
5/5

s=(x^y)^cin

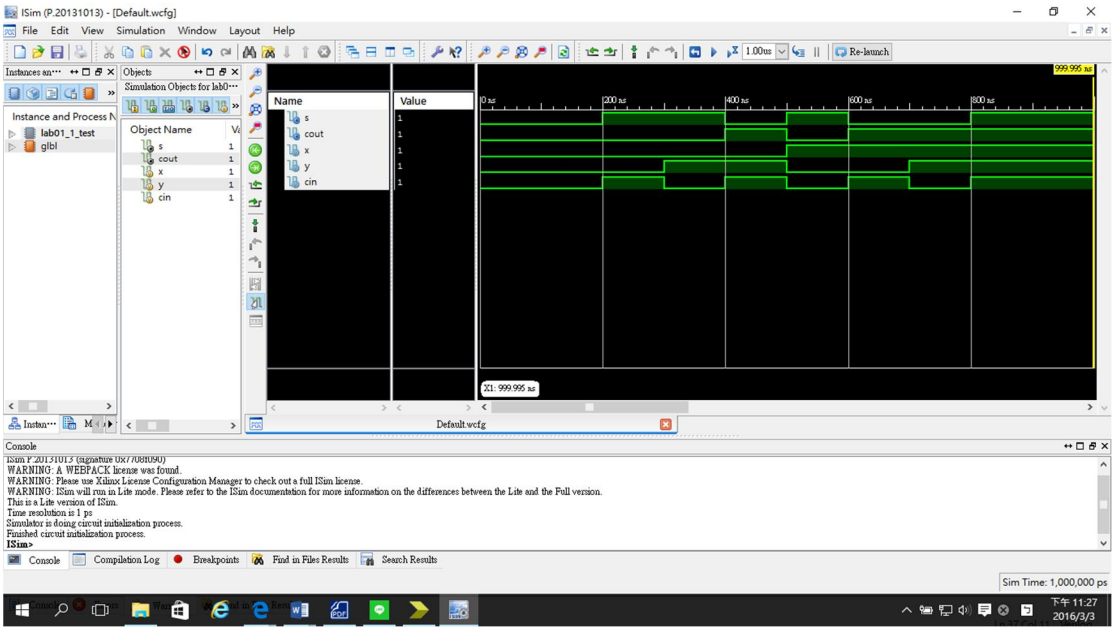
cout=((x^y)&cin)|(x&y)

logic diagram

3/3



The Final Result:



Discussion:

1. 第一次模擬時，Value 欄位出現”x”、”z”錯誤訊息，原來是點錯模擬的檔案，要選擇 Verilog Test Fixture 而不是 Verilog Module。 5/5
2. x=0 y=0 cin=0 -> s=0 cout=0,
   x=0 y=0 cin=1 -> s=1 cout=0,
   x=0 y=1 cin=0 -> s=1 cout=0,
   x=0 y=1 cin=1 -> s=0 cout=1,
   x=1 y=0 cin=0 -> s=1 cout=0,
   x=1 y=0 cin=1 -> s=0 cout=1,
   x=1 y=1 cin=0 -> s=0 cout=1,
   x=1 y=1 cin=1 -> s=1 cout=1。

Discussion 不是用來貼輸出的，請簡述自己實作過程。

2 Design a single digit decimal adder with input A(a3a2a1a0), B(b3b2b1b0), Cin(ci), and output S(s3s2s1s0) and Cout(co).

Design Specification 2/2

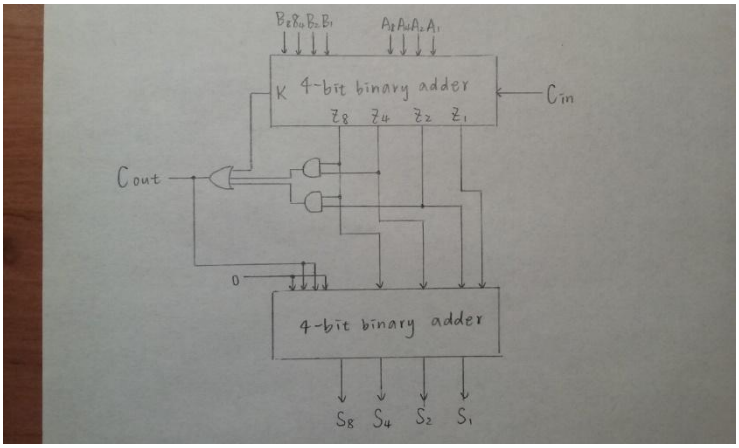
Input:A[3:0],B[3:0],Cin

Output: Cout[3:0],S[3:0]

Wire:z[3:0],K0

block diagram:

你畫的是Logic diagram block diagram 指4bits full adder



5/5

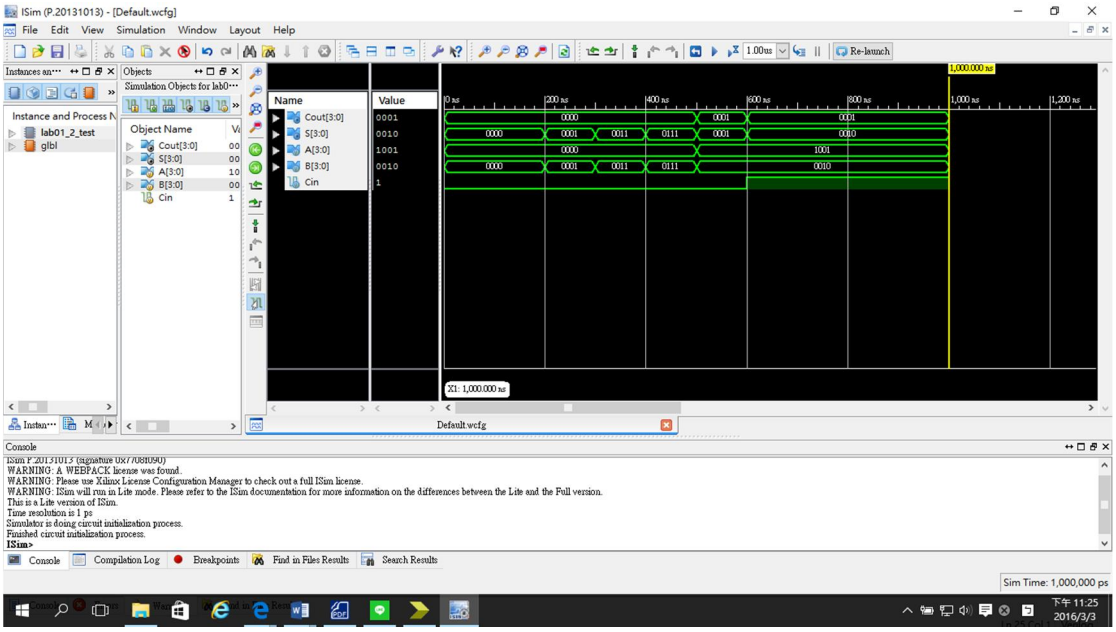
Design Implementation

5/5

logic function:

Cout[0]=K0|(z[3]&z[2])|(z[3]&z[1])

The Final Result:



Discussion:

5/5

Discussion 不是用來貼輸出的，請簡述自己實作過程，下次請注意。

A=0000 B=0000 Cin=0 -> S=0000 Cout=0000,

A=0000 B=0001 Cin=0 -> S=0001 Cout=0000,

A=0000 B=0011 Cin=0 -> S=0011 Cout=0000,

A=0000 B=0111 Cin=0 -> S=0111 Cout=0000,

A=1001 B=0010 Cin=0 -> S=0001 Cout=0001,

A=1001 B=0010 Cin=1 -> S=0010 Cout=0001,

3 (Bonus) Design a 2-to-4-line decoder with enable (input in[1:0], enable en and output d[3:0]). 2/2

3.1 Logic equation,

3.2 Logic schematic,

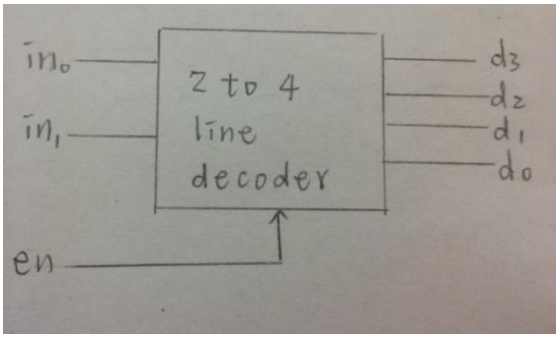
3.3 Verilog RTL representation with verification.

Design Specification

Input:in[1:0],en

Output:d[3:0]

block diagram



Design Implementation

logic function:

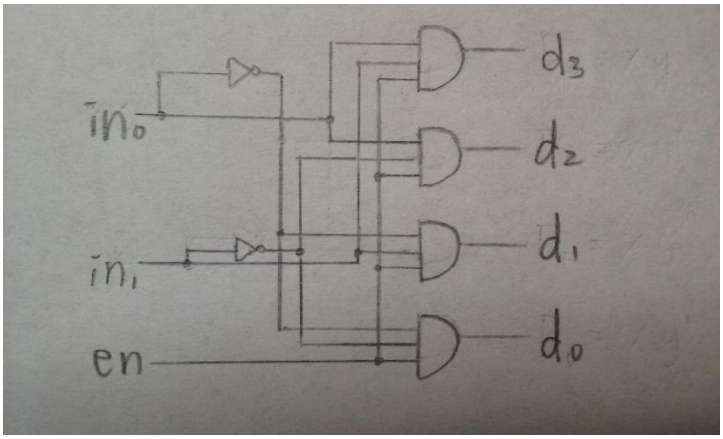
d[3]=en&in[0]&in[1]

d[2]=en&in[0]&(~in[1])

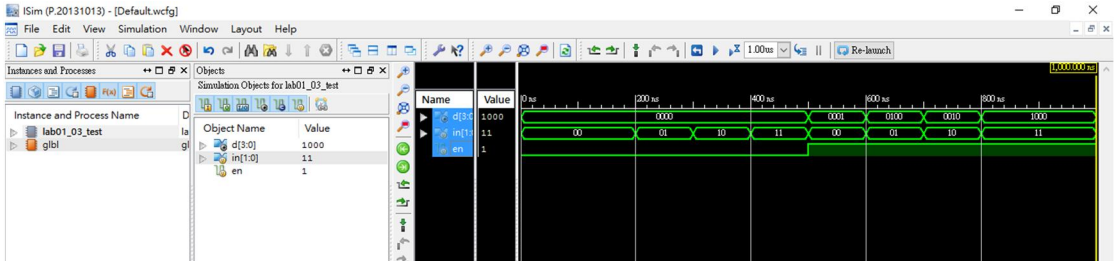
d[1]=en&(~in[0])&in[1]

d[0]=en&(~in[0])&(~in[1])

logic diagram:



The Final Result:



Discussion:

當 enable(en)=0 時，output(d)不受 input(in)影響，其值皆為 1;當 enable(en)=1 時 output(d)受 input(in)影響:in=00 -> d=0001,in=01 -> d=0100,in=10 -> d=0010,in=11 -> d=1000。

Conclusion:

第一次學習 Verilog，對於其與 C 語言的差異有些不習慣，所以花了很長的時間去熟悉，一開始只會一步一步按照講義指示進行，甚至不太清楚自己在做什麼，但慢慢摸索後漸漸找到了方向，最後完成時覺得相當有成就感，期望未來的實驗能更加順利!