EE3450 Hw5 - Question 4 (5.20)

總分 6/6

Chapter 5 : Large and Fast: Exploiting Memory Hierarchy & Virtual Memory

0 分，共 0 分

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Question 4 (5.20) 6 分，共 6 分

[5.3] means you should have read Section 5.3. Under the Covers, to help you solve this exercise

In this exercise, we will examine how replacement policies affect miss rate. Assume a two-way set associative cache with four 4-byte blocks. Consider the following address sequence: 0, 1, 2, 3, 4, 5, 6, 7, 0, 1, 2, 3, 4, 5, 6, 7, 0.

1. [5.4] It is possible to have an even greater cache hierarchy than 2-levels? Given the processor above with a 2-level, direct-mapped cache. A designer want to add a third-level cache that takes 50 cycles to access and will have a 1.3% miss rate.

✓ 1. [5.4, 5.8] Assuming an LRU (most recently used) replacement policy, which accesses are hit? * 3/3

- [ ] 0
- [x] 1 ✓
- [x] 2 ✓
- [x] 3 ✓
- [ ] 4
- [x] 5 ✓
- [x] 6 ✓
- [x] 7 ✓
- [x] 0 (2nd) ✓
- [x] 1 (2nd) ✓
- [x] 2 (2nd) ✓
- [x] 3 (2nd) ✓
- [x] 4 (2nd) ✓
- [x] 5 (2nd) ✓
- [x] 6 (2nd) ✓
- [x] 7 (2nd) ✓
- [x] 0 (3nd) ✓
- [ ] No hit

✓ 2. [5.4, 5.8] Assuming an MRU (most recently used) replacement policy, which accesses are hit? * 3/3

- [ ] 0
- [x] 1 ✓
- [x] 2 ✓
- [x] 3 ✓
- [ ] 4
- [x] 5 ✓
- [x] 6 ✓
- [x] 7 ✓
- [x] 0 (2nd) ✓
- [x] 1 (2nd) ✓
- [x] 2 (2nd) ✓
- [x] 3 (2nd) ✓
- [x] 4 (2nd) ✓
- [x] 5 (2nd) ✓
- [x] 6 (2nd) ✓
- [x] 7 (2nd) ✓
- [x] 0 (3nd) ✓
- [ ] No hit