EE3450 Hw5 - Question 3-2 (5.12.2)

總分 3/3

Chapter 5 : Large and Fast: Exploiting Memory Hierarchy & Virtual Memory

0 分，共 0 分

Email Address *

oliverfeaqr01@gmail.com

Name *

吳柏澄

Student ID *

106061235

Question 3-2 (5.12.2) 3 分，共 3 分

[5.3] means you should have read Section 5.3. Under the Covers, to help you solve this exercise

Multilevel caching is an important technique to overcome the limited amount of space that a first-level cache can provide while still maintaining its speed. Consider a processor with the following parameter:

Base CPI, No Memory Stalls	1.5
Processor Speed	2 GHz
Main Memeory Access Time	100ns
1-Level Cache Miss Rate per Instruction	7%
2-Level Cache, Direct-Mapped Speed	12 cycles
Miss Rate with 2-Level Cache, Direct-Mapped	3.5%
2-Level Cache, 8-Way Set Associative Speed	28 cycles
Miss Rate with 2-Level Cache, 8-way Set Associative	1.5%

Notice the extent to which an L2 cache can hide the effects of a slow memory.

1. [5.4] It is possible to have an even greater cache hierarchy than 2-levels? Given the processor above with a 2-level, direct-mapped cache. A designer want to add a third-level cache that takes 50 cycles to access and will have a 1.3% miss rate.
(Round off to the 2nd decimal place)

✓ Calculate the CPI for the processor. * 3/3

2.47 ✓