EE3450 Hw5 - Question 3-1 (5.12.1)

總分 18/18

Chapter 5 : Large and Fast: Exploiting Memory Hierarchy & Virtual Memory

0 分，共 0 分

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Question 3-1 (5.12.1)

18 分，共 18 分

[5.3] means you should have read Section 5.3. Under the Covers, to help you solve this exercise

Multilevel caching is an important technique to overcome the limited amount of space that a first-level cache can provide while still maintaining its speed. Consider a processor with the following parameter:

Base CPI, No Memory Stalls	1.5
Processor Speed	2 GHz
Main Memeory Access Time	100ns
1-Level Cache Miss Rate per Instruction	7%
2-Level Cache, Direct-Mapped Speed	12 cycles
Miss Rate with 2-Level Cache, Direct-Mapped	3.5%
2-Level Cache, 8-Way Set Associative Speed	28 cycles
Miss Rate with 2-Level Cache, 8-way Set Associative	1.5%

Notice the extent to which an L2 cache can hide the effects of a slow memory.
(Round off to the 2nd decimal place)

1. [5.4] Calculate the CPI for the processor in the table using only a 1-level cache. * 3/3

15.5

2. [5.4] How does the number change if main memory access time double? * 3/3

29.5

3. [5.4] Calculate the CPI for the processor in the table using a 2-level direct-mapped cache. * 3/3

2.83

4. [5.4] How does the number change if main memory access time double? * 3/3

3.32

5. [5.4] Calculate the CPI for the processor in the table using a 2-level 8-way set associative cache. * 3/3

3.67

6. [5.4] How does the number change if main memory access time double? * 3/3

3.88