EE3450 Hw5 - Question 2 (5.7)

總分 6/6

Chapter 5 : Large and Fast: Exploiting Memory Hierarchy & Virtual Memory

0 分，共 0 分

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Question 2 (5.7) 6 分，共 6 分

[5.3] means you should have read Section 5.3. Under the Covers, to help you solve this exercise

Consider the following program and cache behaviors.

Data reads per 1,000 instruction	Data writes per 1,000 instruction	Instruction cache miss rate	Data cache miss rate	Block Size (bytes)
250	100	0.30%	2%	64

1. [5.3, 5.8] Suppose a CPU with a write-through, write-allocate cache achieves a CPI of 2. What are the read and write bandwidths (measured by bytes per cycle) between RAM and the cache? Assume each miss generates a request for one block.
(Round off to the 2nd decimal place)

Hint : Read bandwidth include: (1) Miss in I$ (2) miss in read miss in D$ (3) miss in write miss in D$
Write-allocate will make a read request to RAM when write miss.

✓ Read bandwidth? (bytes/cycle) * 3/3

0.32 ✓

Hint : Write bandwidth include the miss in write miss
Write-through only write a word(4 bytes) when write miss

✓ Write bandwidth? (bytes/cycle) * 3/3

0.2 ✓