EE3450 Hw5 - Question 1 (5.5)

總分 11/11

Chapter 5 : Large and Fast: Exploiting Memory Hierarchy & Virtual Memory

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0 分，共 0 分

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Question 1 (5.5) 11 分，共 11 分

[5.3] means you should have read Section 5.3. Under the Covers, to help you solve this exercise

For direct-mapped cache design with a 64-bit address, the following bits of the address are used to access the cache.

Tag	Index	Offset
63-22	21-12	11-0

✓ 1. [5.3] What is the cache block size (in KB)? * 3/3

4 ✓

✓ 2. [5.3] How many blocks does the cache have? * 3/3

1024 ✓

✓ 3. [5.3] What is the ratio between total bits required for such a cache implementation over the data storage bits?(Round off to the 2nd decimal place) * 3/3

1.00 ✓

Beginning from power on, the following byte-addressed cache references are recorded.

```
Address
0x1fffff48
0x1fffff50
0x1fffff58
0x10034dc4
0x0ffe744c
0x10034db4
0x10034da4
0x10034dac
0x10033ee4
0x3004d978
```

✓ 4. [5.3] What is the hit ratio?(Round off to the 2nd decimal place) * 2/2

0.50 ✓