EE3450 Hw5 - Question 1 (5.5)

總分 11/11



Chapter 5: Large and Fast: Exploiting Memory Hierarchy & Virtual Memory

電子郵件地址 *		
oliverfeaqr01@gmail.com		
	0分, 共0分	
Email Address *		
oliverfeaqr01@gmail.com		
Name *		
吳柏澄 		
Student ID *		
106061235		
Question 1 (5.5)	11分, 共11分	
[5.3] means you should have read Section 5.3. Under the Covers, to help you solve this exercise		

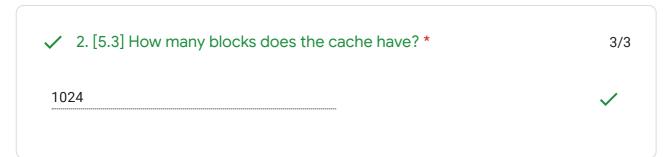
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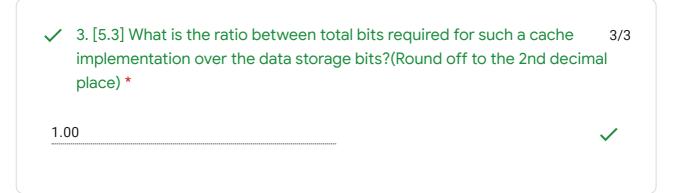
For direct-mapped cache design with a 64-bit address, the following bits of

the address are used to access the cache.

Tag	Index	Offset
63-22	21-12	11-0

1. [5.3] What is the cache block size (in KB)? *	3/3
4	✓





Beginning from power on, the following byte-addressed cache references are recorded.

Address 0x1fffff48 0x1fffff50 0x1fffff58 0x10034dc4 0x0ffe744c 0x10034db4 0x10034da4 0x10034dac 0x10034dac 0x10033ee4 0x3004d978

4. [5.3] What is the hit ratio?(Round off to the 2nd decimal place) *	2/2
0.50	~

這份表單是在 清華大學 中建立。

Google 表單