EE3450 Hw1 - Question 4 - 3

總分 6/6

Chapter 1 Computer Abstraction and Technology

0 分，共 0 分

Email Address *

zxc36mn999947@gmail.com

Name *

陳彥文

Student ID *

106061242

Question 4 - 3 (1.9.3)

6 分，共 6 分

Section 1.6, 1.8

Assume for arithmetic, load/store, and branch instructions, a processor has CPIs of 1, 12, and 5, respectively. Also assume that on a single processor a program requires the execution of 2.56E+9 arithmetic instructions, 1.28E+9 load/store instructions, and 256 million branch instructions. Assume that each processor has a 2 GHz clock frequency. Assume that, as the program is parallelized to run over multiple cores, the number of arithmetic and load/store instructions per processor is divided by 0.7 x p (where p is the number of processors) but the number of branch instructions per processor remains the same.

✓ To what should the CPI of load/store instructions be reduced in order for a single processor to match the performance of four processors using the original CPI values? (Round off to the 2nd decimal place) 6/6

3 ✓